Errata

Title & Document Type: 5005B Signature Multimeter Operating Manual

Manual Part Number: 05005-90015

Revision Date: September 1983

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

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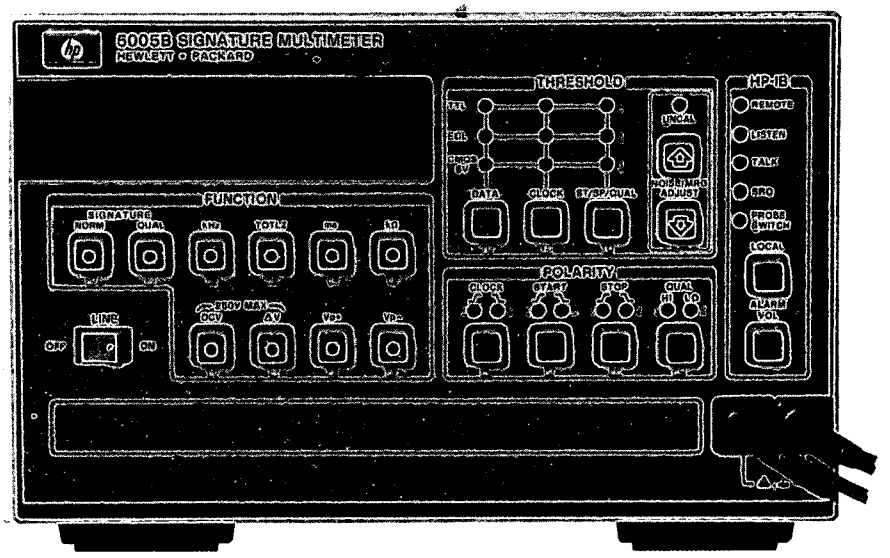
Agilent Technologies

OPERATING AND SERVICE MANUAL

DESIGNED FOR HP-IB SYSTEMS

5005B

Signature Multimeter



HEWLETT PACKARD

HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

5005B

Signature Multimeter

SERIAL PREFIX: 2324A

This manual applies to Serial Prefix 2324A, unless accompanied by a Manual Change Sheet indicating otherwise.

MANUAL PART NUMBER 05005-90015
Mircofiche Part Number 05005-90016

Printed SEPTEMBER 1983

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WARNING

THE SERVICE INFORMATION IS OFTEN USED WITH POWER SUPPLIED AND PROTECTIVE COVERS REMOVED FROM THE 5005B. ENERGY AVAILABLE AT MANY POINTS MAY, IF CONTACTED, RESULT IN PERSONAL INJURY.

WARNING

LINE VOLTAGE IS EXPOSED WITHIN THE 5005B EVEN WHEN THE LINE SWITCH IS SET TO OFF. REMOVAL OF THE POWER CORD IS NECESSARY TO FULLY UNPOWER THE 5005B.

WARNING

ALL TROUBLESHOOTING PROCEDURES REQUIRE INTERNAL ACCESS TO THE INSTRUMENT WITH THE PROTECTIVE COVERS REMOVED. THESE PROCEDURES SHOULD BE PERFORMED ONLY BY SERVICE-TRAINED PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED.

WARNING

BEFORE SWITCHING ON THIS INSTRUMENT, THE PROTECTIVE EARTH TERMINAL OF THIS INSTRUMENT MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE (MAINS) POWER CORD. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE EARTH (GROUNDING) CONDUCTOR.

WARNING

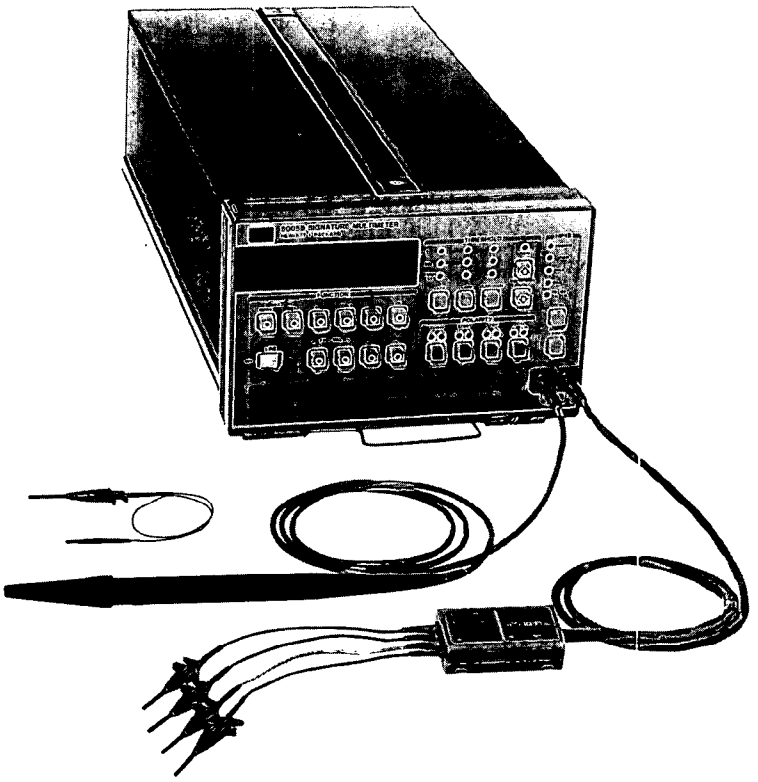
BEFORE THE INSTRUMENT IS SWITCHED ON, ALL PROTECTIVE EARTH TERMINALS, EXTENSION CORDS, AUTO TRANSFORMERS, AND DEVICES CONNECTED TO IT SHOULD BE CONNECTED TO A GROUNDED SOCKET. ANY INTERRUPTION OF THE PROTECTIVE EARTH GROUNDING WILL CAUSE A POTENTIAL SHOCK HAZARD THAT COULD RESULT IN PERSONAL INJURY.

WARNING

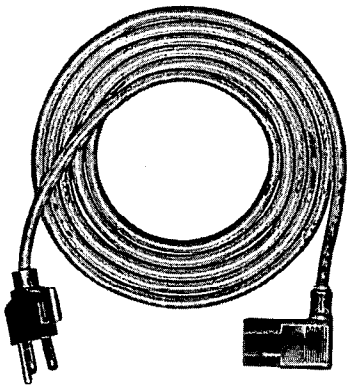
THE GROUND TEST LEADS ON THE POD AND DATA PROBE ARE TIED TO THE CHASSIS GROUND OF THE INSTRUMENT AND SHOULD NOT BE CONNECTED TO A VOLTAGE OTHER THAN GROUND FOR MEASUREMENTS.

WARNING

ONLY FUSES WITH THE REQUIRED RATED CURRENT AND SPECIFIED TYPE SHOULD BE USED. DO NOT USE REPAIRED FUSES OR SHORT-CIRCUITED FUSE-HOLDERS. TO DO SO COULD CAUSE A SHOCK OR FIRE HAZARD.



5005B SIGNATURE MULTIMETER AND EQUIPMENT SUPPLIED



POWER CORD PART NO. 8120-1521

Figure 1-1. Model 5005B Signature Multimeter and Power Cable

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This manual contains the information necessary to install, operate, and program the Hewlett-Packard Model 5005B Signature Multimeter. The multimeter with its supplied accessories is shown in *Figure 1-1*.

1-3. MANUAL SUMMARY

1-4. This manual is divided into eight sections, each covering a particular topic for the operation, programming, and servicing of the HP 5005B. The topics by section number are:

SECTION I, GENERAL INFORMATION. Provides the instrument specifications, instrument identification, accessories and recommended test equipment.

SECTION II, INSTALLATION. Provides information about initial inspection, preparation for use, storage and shipment.

SECTION III, OPERATION. Provides information about operating characteristics, panel features, Operator's Check, operating instructions, measurement procedures, and programming via the Hewlett-Packard Interface Bus.

SECTION IV, PERFORMANCE TESTS. Provides abbreviated procedures for operational verification which give the operator a high degree of confidence that the 5005B is operating properly.

SECTION V, ADJUSTMENTS. Provides the procedures and adjustment locations required to properly maintain the instrument operating characteristics within specifications.

SECTION VI, REPLACEABLE PARTS. Provides ordering information for all replaceable parts and assemblies within the instrument.

SECTION VII, MANUAL CHANGES. This section is reserved for manual change information which effectively "backdates" the technical areas of the manual to apply to older instruments.

SECTION VIII, SERVICE. This section provides the instrument theory of operation, troubleshooting information, repair techniques, and schematic diagrams.

1-5. SPECIFICATIONS

1-6. The specifications for the 5005B are listed in *Table 1-1*. These specifications are the performance standards or limits against which the 5005B can be tested.

1-7. DESCRIPTION

1-8. The 5005B Signature Multimeter is an HP-IB programmable multipurpose instrument for troubleshooting electronic logic circuits to the component level. The 5005B provides the following measurement modes: frequency, totalize, time interval, DC voltage, voltage difference, positive or negative peak voltage, and resistance.

1-9. The 5005B can also display digital "signatures" of logic circuits. This method of troubleshooting is called "signature analysis". Typically, a logic product designed for signature analysis troubleshooting will have a programmed controller and a stored or externally-provided test program which can exercise most of the unit.

Table 1-1. 5005B Specifications

SIGNATURE

Display: 4 digits. Characters 0-9, ACFHPU.

Fault detection accuracy: 100% probability of detecting single-bit errors; 99.998% probability of detecting multiple-bit errors.

Minimum gate length: 1 clock cycle (1 data bit) between START and STOP.

Maximum gate length: no limit.

Minimum timing between gates: 1 clock cycle between STOP and START.

Data probe timing:
Setup time: 10 ns (data to be valid at least 10 ns before selected clock edge.)
Hold time: 0 ns (data to be held until occurrence of selected clock edge.)

START, STOP, QUAL timing:
Setup time: 20 ns (signals to be valid at least 20 ns before selected clock edge.)
Hold time: 0 ns (signals to be held until occurrence of selected clock edge.)

CLOCK timing:
Maximum clock frequency: 25 MHz.
Minimum pulse width: 15 ns in high or low state.

Supplemental characteristics
Front panel indicators: flashing GATE light indicates detection of valid START, STOP, CLOCK conditions. Flashing UNSTABLE light indicates a difference between 2 successive signatures, and possible intermittent faults. Edge select lights indicate active edges for START, STOP, CLOCK and QUAL inputs.
Qualify mode: allows clock data qualification by an external signal.
DATA probe input impedance: 50 kΩ to the average value of "0" and "1" threshold settings (±6V max); 15 pF.
START, STOP, CLOCK, QUAL input impedance: 100 kΩ; 15 pF.

FREQUENCY

Display: 5 digits.
Ranges: 100 kHz, 1 MHz, 10 MHz, 50 MHz, autoranged.
Resolution: 1 LSD (1 Hz on 100 kHz range).
Accuracy: ±0.01% of reading ±1 count.

Supplemental characteristics
Minimum pulse width: 10 ns in high or low state.
Gate time: 1 s, fixed.
Input impedance: 50 kΩ to the average value of "0" and "1" threshold settings (±6V max); 15 pF.

TOTALIZE

Display: 5 digits.

Range: 0-99,999 counts.

Resolution: 1 count.

Supplemental characteristics
Maximum input frequency: 50 MHz, with a minimum pulse width of 10 ns, and minimum pulse separation of 10 ns.

Minimum START/STOP pulse width: 20 ns.

Accuracy: *±0 counts. (Start must precede first counted pulse by 50 ns minimum, Stop must follow last counted pulse by 50 ns minimum, otherwise ±2 Counts).*

DATA input impedance: 50 kΩ to the average value of "0" and "1" threshold settings (±6V max); 15 pF.
START, STOP input impedance: 100 kΩ; 15 pF.

TIME INTERVAL

Display: 5 digits.

Ranges: 10 ms, 100 ms, 1 s, 10 s, 100 s, autoranged.

Resolution: 1 count (100 ns on 10 ms range).

Accuracy: ±0.01% of reading ±2 count.

Supplemental characteristics
Minimum START/STOP pulse width: 20 ns.
START, STOP input impedance: 100 kΩ; 15 pF.

RESISTANCE

Display: 4 or 5 digits, depending on range.

Ranges: 30 kΩ, 300 kΩ, 1 MΩ, 3 MΩ, 10 MΩ, autoranged.

Accuracy: (at 15°C-30°C ≤80% RH).

RANGE	FULL SCALE	ACCURACY	DISPLAY RESOLUTION
30 kΩ	29.999 kΩ	±1% of reading ±2 Ω	1 Ω
300 kΩ	299.99 kΩ	±1% of reading	10 Ω
1 MΩ	999.9 kΩ	±1% of reading	100 Ω
3 MΩ	2999. kΩ	±10% of reading	1 kΩ
10 MΩ	10000. kΩ	±10% of reading	10 kΩ

Supplemental characteristics
Input impedance: 20 kΩ to +2V.

Table 1-1. 5005B Specifications (Continued)

DC VOLTAGE

Display: 4½ digits.

Ranges: ±25V, ±250V, autoranged; referenced to earth ground.

Accuracy: (at 15°C-30°C ≤80% RH).

RANGE	ACCURACY	RESOLUTION
25V	±0.1 % of reading ± 2mV	1mV
250V (<100V)	±0.25% of reading ±20mV	10mV
250V (≥100V)	±0.25% of reading ±20mV	100mV

Supplemental characteristics
Input impedance: 10 MΩ

DIFFERENTIAL VOLTAGE

Reading: Reads input voltage present at the probe and displays difference between it and voltage at the time ΔV key was depressed.

Specifications: Same as for DCV, above. Voltage range is determined by larger of 2 compared voltages.

Supplemental characteristics
Same as for DCV, above.

PEAK VOLTAGE

Display: 3½ digits.

Range: 0 - ±12Vp.

Resolution: 50mV.

Accuracy: ±2% of reading ±5% of p-p signal ±100mV.

Supplemental characteristics
Minimum peak duration: 10 ns.
Maximum time between peaks: 50 ms.
Input impedance: 100 kΩ; 15 pF.

LOGIC THRESHOLDS

Preset thresholds: (All levels ±0.2V).

FAMILY	DATA "1"	DATA "0"	CLOCK-ST-SP-QL
TTL	2.0V	0.8V	1.4V
ECL	-1.1V	-1.5V	-1.3V
CMOS	3.5V	1.5V	2.5V

Adjustable thresholds: Each preset threshold can be adjusted.
Range: ±12.5V, in 50mV steps.
Accuracy: ±2% of setting, ±200mV.

Operating characteristics
Logic threshold circuitry is operative during NORM, QUAL, kHz, TOTLZ and ms measurements.

GENERAL

Data probe tip: Acts as high-speed logic probe in the NORM, QUAL, kHz and TOTLZ modes. Lamp indicates high, low, bad-level and pulsing states. Minimum detected pulse width is 10 ns.

Data probe protection:
Continuous overload:
DCV, ΔV, kΩ modes only: ±250V AC/DC.
All other modes: ±150V AC/DC, 20V rms at input frequencies > 2 MHz.
Intermittent overload: ±250V AC/DC, up to 1 min, for all modes.

Timing pod protection:
Continuous overload: ±100V AC/DC, 20V rms at input frequencies > 2 MHz.
Intermittent overload: ±140V AC/DC, up to 1 min.

Operating temperature: 0°C to +55°C.

Operating humidity: 95% RH at +40°C, except as specified otherwise for DCV, ΔV and kΩ modes.

Power: Selectable 100V, 120V, 220V, or 240V AC line (+5%-10%), 48-66 Hz. 70 VA maximum.

Weight: Net: 12 lbs.

Size: 5¾ in × 8⅜ in × 17 in (43.2 mm high × 146 mm wide × 213 mm deep).

*__Specifications__ describe the instrument's warranted performance. *Supplemental characteristics* (shown in italics) are intended to provide information useful in applying the instrument, but are non-warranted performance parameters.

1-10. ACCESSORIES SUPPLIED

1-11. The accessories supplied with the 5005B are shown in *Figure 1-1*. Their description and part number are given below:

a. Depending on the customer's country, the line power cable supplied has one of six appropriate line (mains) connectors. Refer to *Figure 2-2*, Power Cable HP Part Numbers Versus Mains Plugs Available, for the part number of the correct cable.

b. Five detachable "grabber" test connectors are supplied with the 5005B. Their part number is 10230-62101. Refer to Section III for description and use.

c. One ground lead for the data probe is supplied with the 5005B. Its part number is 05005-60116. One data probe tip cover is supplied. Its part number is 00547-40005.

1-12. INSTRUMENT AND MANUAL IDENTIFICATION

1-13. The instrument serial number is located just below the power input module on the rear panel. The serial number is in the form: 0000A00000. The first four digits and the letter are the serial prefix. The last five digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-14. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a yellow Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-15. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-16. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

1-17. SAFETY CONSIDERATIONS

1-18. The 5005B is a Safety Class 1 instrument provided with a protective earth terminal. Safety information pertinent to the operation and servicing of this instrument is included in appropriate sections of this manual.

1-19. Safety Symbols

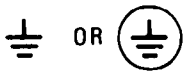
NOTE

The symbol ⚠ (ATTENTION), which appears on the front panel of the instrument, indicates that the user should refer to the instruction manual before operating in order to avoid possible damage to the instrument. Within the manual, information relating to the ATTENTION symbol will be identified with a ⚠ symbol in the margin.

1-20. The following safety symbols are used on equipment and in manuals:

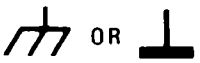
Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with the symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.



Frame and chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current.

Direct current.

Alternating or direct current.

The WARNING signal denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

1-21. RECOMMENDED TEST EQUIPMENT

1-22. Equipment required to maintain the HP Model 5005B is listed in *Table 1-2.* Other equipment can be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-2. Recommended Test Equipment

Equipment	Required Characteristics	Used For				Recommended HP Model
		Adjustments	Op. Verification	Performance Tests	Troubleshooting	
Sig. Multimeter	See *Table 1-1*				X	5005B
Digital Voltmeter	+0.001% acc.	X		X	X	3455A
2 Pulse Generators	50MHz Rate <5ns transition time			X		8012A
Pulse Generator	Presettable single-shot bursts			X		8011A/W OPT 001
Universal Counter	100MHz+TI 1ns Resolution			X		5370A
Universal Counter	100MHz			X		5316A
Pulse Generator	100MHz Rate <2ns transition time	X				8007B
Power Supply	±300VDC			X		6209B
Power Supply	0-30 VDC, ADJ 10mV Resolution			X		6216A
Oscilloscope	100MHz BW	X			X	1740A
Oscilloscope	275MHz BW			X		1725A
Function Generator	0.1Hz to 1MHz		X			3312A
Function Generator	50MHz			X		8165A
Logic Lab Breadboard				X		5035T
Microprocessor Lab			X*			5036A
Probe Set					X	5022A
Tuning Wand	Ceramic Wand	X				8710-0033
Controller Calculator	HP-IB Compatible		X	X		HP 85F†

*Any instrument with HP compatible digital signature analysis capability can be substituted here.
†HP 85F consists of the following:

Controller Calculator	HP 85A
I/O ROM	00085-15003
ROM DRAWER	HP 82936A
HP-IB INTERFACE CARD/CABLE	HP 82937A

SECTION II
INSTALLATION

2-1. INTRODUCTION

2-2. This section contains information for unpacking, inspection, installation and storage.

2-3. UNPACKING AND INSPECTION

2-4. If the shipping carton is damaged, inspect the instrument for visible damage (scratches, dents, etc.). If the instrument is damaged, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately (offices are listed at the back of this manual). Keep the shipping carton and packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for repair or replacement of your instrument without waiting for the claim against the carrier to be settled.

2-5. PREPARATION FOR USE

CAUTION

Before connecting the instrument to ac power lines, be sure that the voltage selector is properly positioned as described below.

2-6. Power Requirements

2-7. The 5005B requires an ac line power source of 100V, 120V, 220V, or 240V, +5%, -10%, 48 to 66 Hz single phase. Power consumption is 35 VA maximum.

2-8. Line Power Module

2-9. The 5005B is provided with a line power module, which contains the main line fuse and a removable printed-circuit board. The printed-circuit board is installed in the line module in one of four positions, to select 100, 120, 220, or 240 Vac operation. Before applying power, verify that the printed-circuit board voltage selector is properly positioned for the desired ac supply voltage and that the correct fuse is installed.

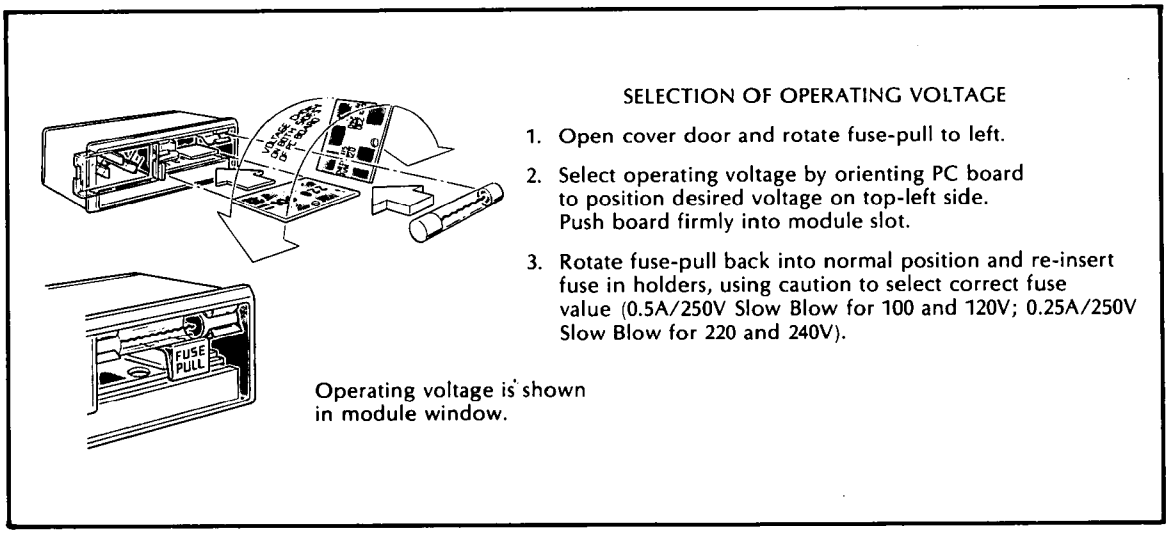


Figure 2-1. Line Voltage Selection

2-10. Selection of Operating Voltage and Main Line Fuse

2-11. Power line connections are selected by the position of the plug-in printed circuit board in the line power module. When the PC board is inserted into the module, the visible markings on the board indicate the configured line voltage. When converting from one line voltage to another, the power cord must be disconnected from the power module to allow the sliding window to be moved, which exposes the fuse and PC board compartment. To replace the main power fuse or change the selected line voltage, perform the following steps. Also see *Figure 2-1*.

1. Remove the power cord, and slide the fuse compartment window to the left.
2. Gently pull the FUSE PULL tab out and to the left. This frees one end of the fuse for easier removal, and allows access to the PC voltage selector board.
3. Select the operating voltage by orienting the PC board such that the desired voltage label appears on the top side and left half of the board. Push the board firmly into the PC board slot, located below the fuse. When fully seated, the configured operating voltage will be the only visible label.
4. Rotate the FUSE PULL tab back to its normal position. Insert the fuse by positioning against the snap-in connectors, and pressing in both ends. Be sure to install the correct fuse value; 0.5A/250V Slow Blow for 100V & 120V operation; 0.25V/250V Slow Blow for 220V & 240V operation.

2-12. Power Cable

2-13. The 5005B is shipped with a three-wire power cable. When the cable is connected to an appropriate ac power source, this cable connects the instrument chassis to earth ground. The type of power cable plug shipped with each instrument depends on the country of destination. Refer to *Figure 2-2* for the part numbers of the power cable and plug configurations available.

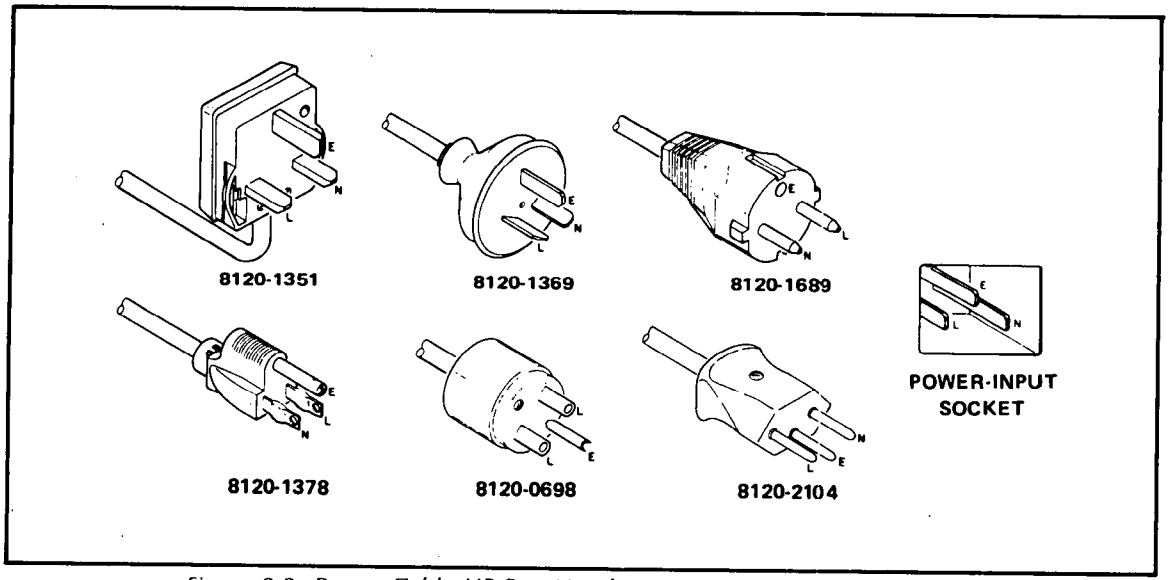


Figure 2-2. Power Cable HP Part Numbers versus Mains Plugs Available

WARNING

BEFORE SWITCHING ON THIS INSTRUMENT, THE PROTECTIVE EARTH TERMINAL OF THIS INSTRUMENT MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE (MAINS) POWER CORD. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE EARTH (GROUNDING) CONDUCTOR.

2-14. HP-IB Interconnections

2-15. HEWLETT-PACKARD INTERFACE BUS. Interconnection data concerning the rear panel HP-IB connector is provided in *Figure 2-3*. This connector is compatible with the HP 10833A/B/C/D cables. (See *Table 2-1* for cable descriptions.) The HP-IB system allows interconnection of up to 15 (including the controller) HP-IB compatible instruments. The HP-IB cables have identical "piggy-back" connectors on both ends so that several cables can be connected to a single source without special adapters or switch boxes. System components and devices may be connected in virtually any configuration desired. There must, of course, be a path from the calculator (or other controller) to every device operating on the bus. As a practical matter, avoid stacking more than three or four cables on any one connector. If the stack gets too large, the force on the stack produces great leverage which can damage the connector mounting. Be sure each connector is firmly (finger tight) screwed in place to keep it from working loose during use.

Table 2-1. HP-IB Cable Descriptions

10833A	1 meter (3.3 ft.)
10833B	2 meters (6.6 ft.)
10833C	4 meters (13.2 ft.)
10833D	0.5 meters (1.6 ft.)

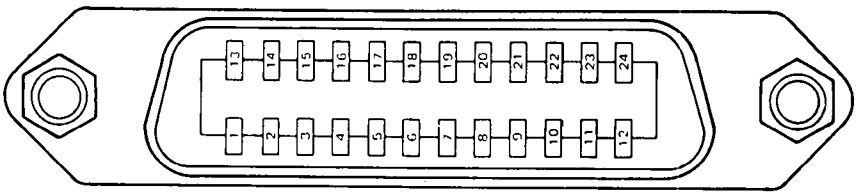
The above symbol when located in the upper corner of a page indicates HP-IB information is contained on that page. This information may be operation, performance, adjustment, or service related.

2-16. CABLE LENGTH RESTRICTIONS. To achieve design performance with the HP-IB, the proper voltage levels and timing relationships must be maintained. If the system cable is too long, the lines cannot be driven properly, and the system will fail to perform properly. Therefore, when interconnecting an HP-IB system, it is important to observe the following rules:

a. The total cable length for the system must be less than or equal to 20 meters (65 feet).

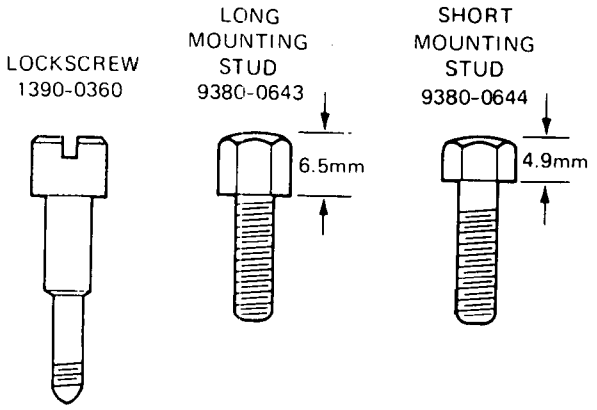
b. The total cable length for the system must be less than or equal to 2 meters (6.6 feet) times the total number of devices connected to the bus.

c. The total number of instruments connected to the bus must not exceed 15.



PIN	LINE	
1	DIO1	
2	DIO2	
3	DIO3	
4	DIO4	
13	DIO5	
14	DIO6	
15	DIO7	
16	DIO8	
5	EOI	
17	REN	
6	DAV	
7	NRFD	
8	NDAC	
9	IFC	
10	SRQ	
11	ATN	
12	SHIELD-CHASSIS GROUND	
18	P/O TWISTED PAIR WITH PIN 6	THESE PINS ARE INTERNALLY GROUNDED
19	P/O TWISTED PAIR WITH PIN 7	
20	P/O TWISTED PAIR WITH PIN 8	
21	P/O TWISTED PAIR WITH PIN 9	
22	P/O TWISTED PAIR WITH PIN 10	
23	P/O TWISTED PAIR WITH PIN 11	
24	ISOLATED DIGITAL GROUND	

The 5005B contains metric threaded HP-IB cable mounting studs as opposed to English threads. Metric threaded HP 10833A, B, C, or D HP-IB cable lockscrews must be used to secure the cable to the instrument. Identification of the two types of mounting studs and lockscrews is made by their color. English threaded fasteners are colored silver and metric threaded fasteners are colored black. DO NOT mate silver and black fasteners to each other or the threads of either or both will be destroyed. Metric threaded HP-IB cable hardware illustrations and part numbers follow.



Logic Levels

The Hewlett-Packard Interface Bus logic levels are TTL compatible, i.e., the negative true logic (1) state is 0.0 Vdc to 0.4 Vdc and the false (0) state is +2.5 Vdc to +4.0 Vdc.

Programming

Refer to Section III, Operation.

Mating Connector

HP 1251-0293; Amphenol 57-30240.

Mating Cables Available

HP 10833A, 1 metre (3.28 ft.)
HP 10833B, 2 metres (6.56 ft.)
HP 10833C, 4 metres (13.12 ft.)
HP 10833D, 0.5 metre (1.64 ft.)

Cabling Restrictions for Standard System

1. A Hewlett-Packard Interface Bus System may contain no more than 1.8 metres (6 ft.) of connecting cable per instrument.
2. The maximum accumulative length of connector cable for any Hewlett-Packard Interface Bus System is 20.0 metres (65.6 ft.)

Figure 2-3. Hewlett-Packard Interface Bus Connections

2-17. HP-IB Talk/Listen Address Switch

2-18. The 5005B provides a rear panel HP-IB instrument address selection switch. This switch determines the mode of remote operation as "TALK ONLY" or "ADDRESSABLE", and selects the HP-IB address. Instructions for changing the address are provided in Section III of this manual.

2-19. HP-IB Description

2-20. A description of the HP-IB is provided in Section III of this manual. A study of this information is necessary if the user is not familiar with the HP-IB concept. Additional information concerning the design criteria and operation of the bus is available in IEEE Standard 488-1978, titled "IEEE Standard Digital Interface for Programmable Instrumentation." See *Figure 2-3.*

2-21. Operational Check

2-22. To determine if the instrument is operating properly, refer to the Operation Verification in Section IV. Contact your nearest HP Sales and Service Office (see manual back cover) for information concerning warranty claims.

2-23. Operating Environment

2-24. TEMPERATURE. The 5005B may be operated in temperatures from 0°C to +55°C.

2-25. HUMIDITY. The 5005B may be operated in environments with humidity up to 80% at 40°C. However, it should be protected from extreme temperatures which cause condensation in the instrument.

2-26. ALTITUDE. The 5005B may be operated at altitudes up to 4,600 meters (15,000 feet).

2-27. STORAGE AND SHIPMENT

2-28. Environment

2-29. The instrument may be stored or shipped in environments within the following limits:

TEMPERATURE	-40°C to +75°C
HUMIDITY	Up to 80% noncondensing
ALTITUDE	7,620 meters (25,000 feet)

2-30. The instrument should also be protected from temperature and humidity extremes which cause condensation within the instrument.

2-31. Packaging

2-32. ORIGINAL PACKAGING. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-33. OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials:

a. Wrap instrument in heavy paper or plastic. (If shipping to Hewlett-Packard office or service center, attach tag indicating type of service required, return address, model number, and full serial number.)

b. Use strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3- to 4-inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

SECTION III
OPERATION

3-1. INTRODUCTION

3-2. This section gives complete operating and programming information for the 5005B Signature Multimeter. Descriptions of all front panel controls, connectors, and indicators, as well as an operator's check, operating instructions, and operator's maintenance, are provided.

3-3. OPERATING CHARACTERISTICS

3-4. The 5005B Signature Multimeter is an HP-IB programmable multipurpose test instrument capable of the following measurements:

Signature Analysis (NORM or QUAL)
Frequency (kHz)
Totalize (TOTLZ)
Time Interval (ms)
Resistance (kΩ)
Voltage (DCV)
Differential Voltage (ΔV)
Positive Peak Voltage (Vp+)
Negative Peak Voltage (Vp-)

3-5. In all digital measurements (Signature Analysis, Frequency, Totalize, and Time Interval), selectable logic thresholds define the logic states for incoming signals. Basic operating characteristics include frequency measurements up to 50 MHz with a fixed one second gate time, time interval measurements down to 100ns, resistance measurements in five autoranges with up to 1 ohm resolution, DC voltage measurements in two autoranges up to ± 250V, and peak voltage measurements up to ±12 volts with 50mV resolution. The operating range, resolution, and accuracy for each individual functional mode are given in the Specifications, *Table 1-1*.

3-6. All of the capabilities of the 5005B, with the exception of Signature Analysis, are standard measurement functions and require little explanation. Operators unfamiliar with Signature Analysis should refer to the description in paragraph 3-11.

3-7. OPERATING INSTRUCTIONS

3-8. Information and instructions for operating the 5005B in both the local and remote modes are provided in this section. The following paragraphs summarize the organization and content of the operating information.

3-9. LOCAL OPERATION. The operating information for local (or manual) operation of the 5005B consists of the following topics:

- *Front and Rear Panel Features.* Consists of *Figures 3-6* through *3-9*, which locate and describe all of the front and rear panel operator controls and indicators.
- *Measurement Procedures.* Consists of *Tables 3-6* through *3-14*, which provide step-by-step operator instructions and keystroke examples for each of the measurement functions.
- *General Operation Information.* Begins with paragraph 3-42, and describes the basic recommended sequence of measurement operations. Provides detailed instructions for selecting the desired input logic family, threshold level, and polarity.
- *Modes of Operation.* Begins with paragraph 3-56, and provides a general description of the capabilities and requirements for each of the labeled key functions.

3-10. REMOTE OPERATION. The remote programming operating instructions begin with paragraph 3-79. A good working knowledge of the local operation of the 5005B is essential for HP-IB programming, as most of the data messages perform the same keystroke-like sequences. Where applicable, program examples are provided. The Remote Operation/Programming instructions describe the following:

- General HP-IB Information
- Bus Compatibility
- Interface Functions
- Bus Messages
- Address Selection
- Error Conditions
- Front Panel HP-IB Status LEDS
- Input Code Format
- Output Format
- Talk Only Mode
- Measurement Triggering in Remote
- Signature Collection
- Command Codes
- Service Request Mask
- Programming Examples

3-11. SIGNATURE ANALYSIS

3-12. Signature Analysis (SA) is a technique for component-level troubleshooting. A Signature Analyzer detects and displays the unique digital signatures associated with the data at nodes in a circuit under test. By comparing these actual signatures to known correct ones, a troubleshooter can quickly backtrace to a faulty node.

3-13. The HP 5005B Signature Multimeter displays a compressed, four digit "fingerprint" or signature of the digital data stream at a logic node. The four character front panel Signature Analysis display presents numbers in a special set of hexadecimal symbols. The 16 special hexadecimal characters used for signature displays are:

3-14. Notice that the final six symbols are not the common hexadecimal symbols "ABCDEF". The seven-segment LED displays used in the 5005B cannot show a "B" or "D" that would appear different from an "8" or "0", respectively. Also, several other symbols could be misinterpreted as another character when viewed upside-down (e.g. E3).

3-15. The special characters presented on the display represent the residue in a CRC (Cyclical Redundancy Code) shift register in the 5005B, after START and STOP signals have been received. The number of data bits between the START and STOP signals can be 1 to ∞ (infinity).

NOTE

No signature appearing on the 5005B display has any particular significance beyond being a correct (expected) signature or an incorrect signature. The number is, however, a residue in the 5005B converted to and displayed in special hexadecimal form.

3-16. SIGNATURE ANALYSIS LITERATURE

3-17. Further Signature Analysis information literature is listed in *Application Note 222-0, An Index to Signature Analysis Publications*. This maintained document lists the description and part number of the available literature concerning Signature Analysis, which can be ordered through the nearest Hewlett-Packard Sales and Service Office.

3-18. DATA PROBE AND TIMING POD HOLDER

3-19. The 5005B provides a (removable) wire holder, located on the lower edge of the front panel, as a convenient place to store the Data Probe and Timing Pod. *Figure 3-1* shows the 5005B Data Probe and Timing Pod in the recommended storage position.

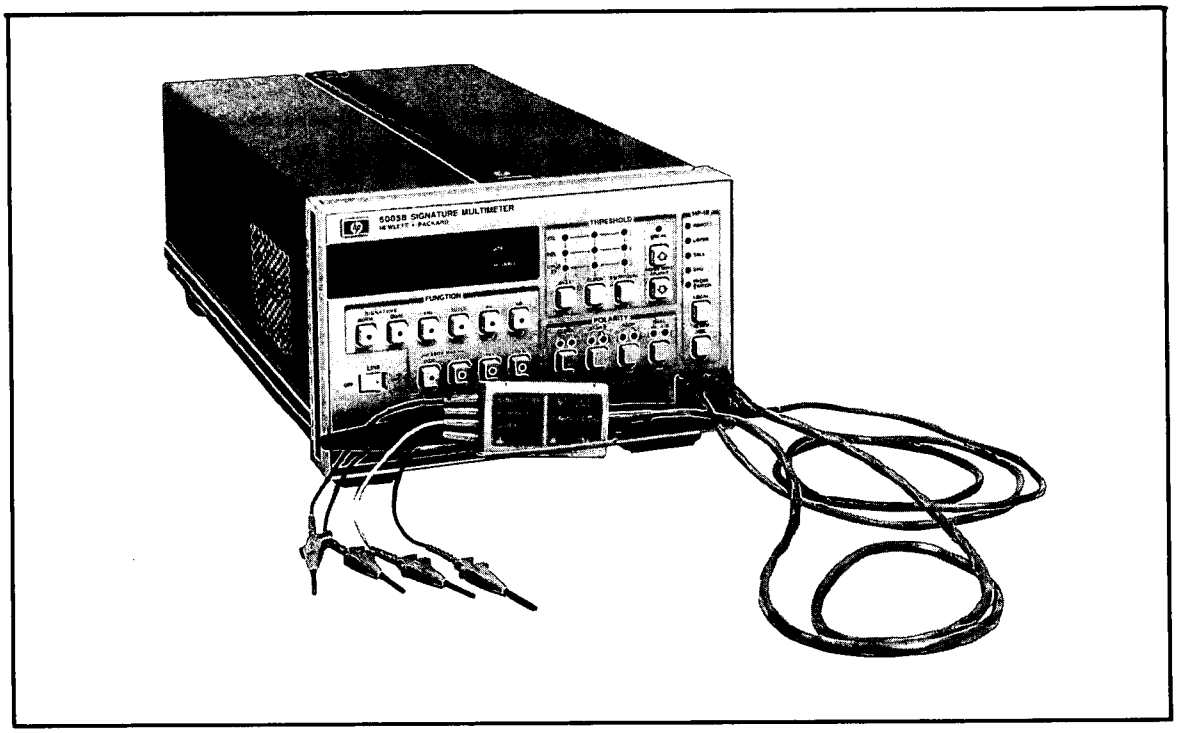


Figure 3-1. Data Probe and Timing Pod Holder

3-20. TEST TERMINAL GRABBER CONNECTIONS

3-21. Five test-terminal grabber connectors are supplied with the 5005B. A grabber can be used on the end of the Timing Pod leads to make reliable electrical connections from the 5005B to the instrument being tested. To connect a grabber to a test lead of the Pod, simply press the grabber on to the lead as shown in *Figure 3-2*. To place a grabber on an IC pin, grasp the grabber and compress the thumbhold. This allows the metal hook to open and be placed on the desired IC pin. To remove the grabber, compress the thumbhold and remove the grabber from the IC pin. A grabber is also provided for the removable ground (⊥) test lead for the Data Probe.

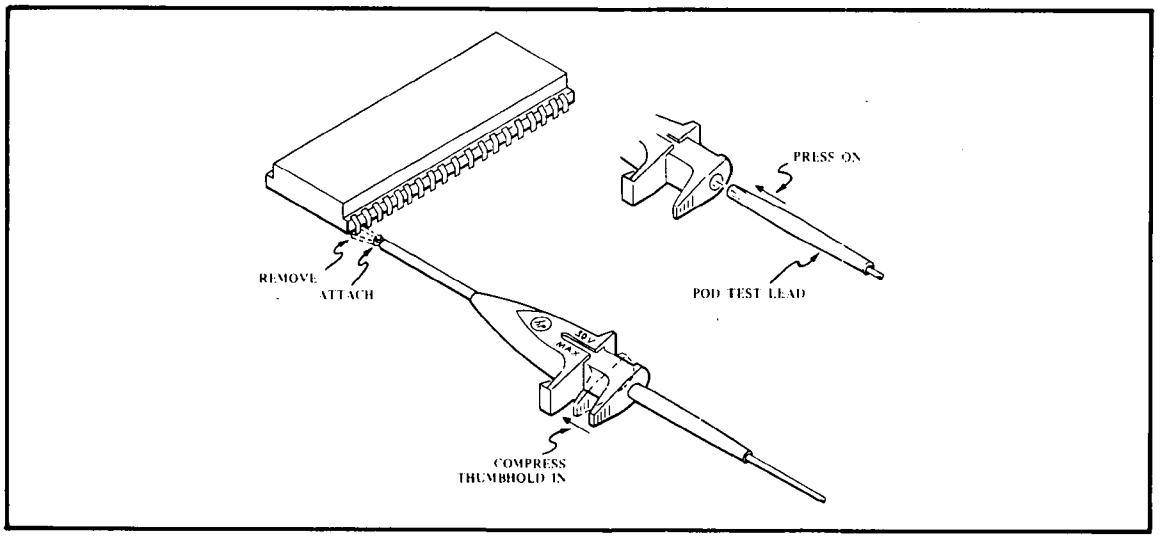


Figure 3-2. Test Terminal Grabber Connections

3-22. TYPICAL CONNECTIONS OF 5005B TO DEVICE UNDER TEST

3-23. *Figure 3-3* shows the 5005B Signature Multimeter connected to another device, taking signatures.

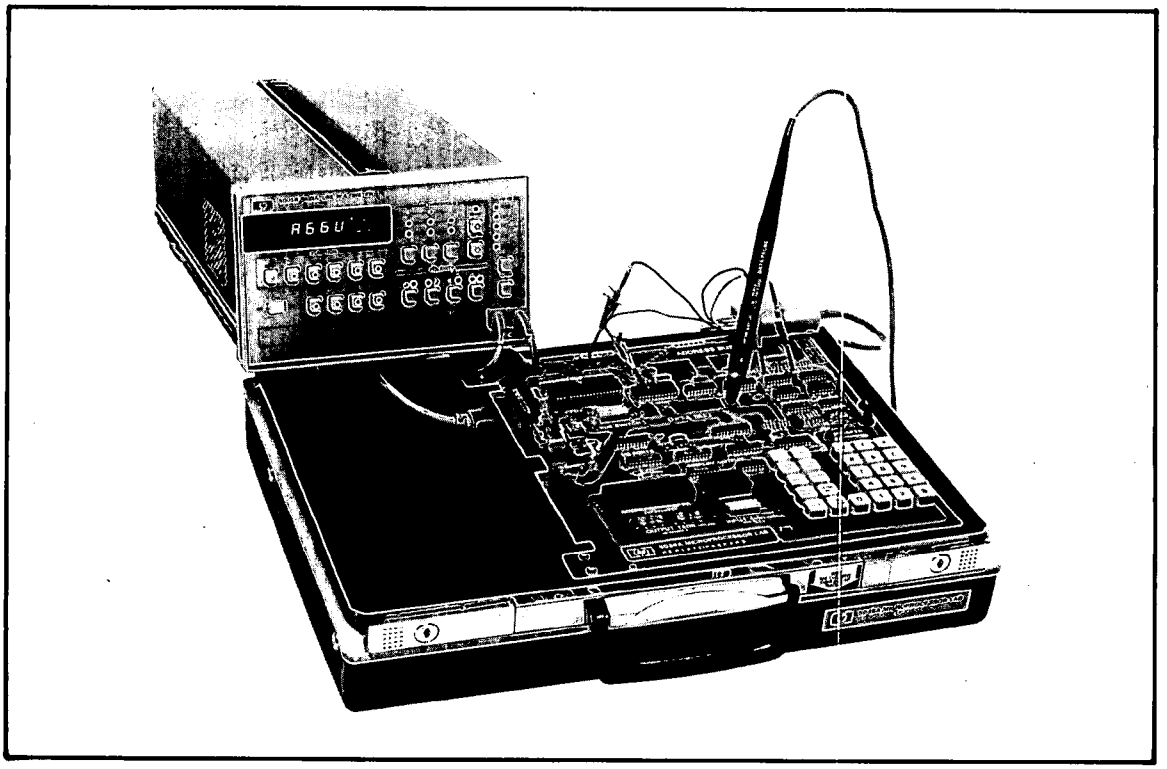


Figure 3-3. Typical Connections of 5005B to Device Under Test

3-24. PANEL FEATURES

3-25. The front and rear panel connectors, indicators, and controls of the 5005B are described in *Figures 3-6, 3-7, 3-8,* and 3-9. These figures locate and describe all operator accessible front and rear panel features.

3-26. MEASUREMENT PROCEDURES

3-27. Recommended measurement procedures for the 5005B are provided in *Tables 3-6* through *3-14*. These procedures are arranged by function mode, and describe in a step-by-step fashion, the keystroke sequence for typical measurement operation.

3-28. OPERATOR'S MAINTENANCE

3-29. The only maintenance the operator should normally perform is the replacement of the primary power line fuse. This fuse is located within the rear panel Line Module Assembly. Refer to Section II, Line Voltage Selection, for instructions on changing the fuse.

CAUTION

Make sure that only fuses with the required rated current, and of the slow-blow type are used for replacement. The use of repaired fuses and the short-circuiting of fuse holders must be avoided.

3-30. OPERATOR'S CHECK

3-31. A procedure to verify the basic operation of the 5005B is provided in *Table 3-5*. The check utilizes the instrument's self-check cycle and visual verification of front panel indications. *No additional equipment is required.*

3-32. POWER-UP SELF-CHECK

3-33. When the 5005B is turned-on, a power-up self-check cycle is automatically started. With no inputs applied to the Data Probe or Timing Pod, the sequence is as follows:

1. After placing the LINE switch from OFF to ON, all the display segments, indicators, and key LEDs on the front panel and display should light, except the GATE and UNSTABLE LEDs which should flash on momentarily.
2. After approximately three seconds, an audible tone should sound, indicating that the 5005B has successfully completed the self-check cycle.
3. After power-up, the rising edge indicators for CLOCK, START, and STOP, the THRESHOLD TTL LEDs, and the NORM key LED should be lighted. The display should have four dashes (center segments) lighted.

3-34. During this cycle, the microprocessor performs a checksum of the internal program in ROM, and a bit pattern is written into and read from RAM. Additionally, a timer test, DVM test, internal counter test, LED test, and a partial check of the D/A converter circuits are performed. A failure during the cycle will cause an "Err15" error message to be displayed, or result in a visibly improper state of the front panel display and indicators (as described above). Errors other than Err15 (such as Err07) could appear momentarily, but should be ignored . Refer to Error Messages, paragraph 3-37.

3-35. QUICK OPERATION TEST

3-36. The following quick operation test can be used to verify other circuits not checked in the power-up self-check routine. The procedure is as follows:

1. Press the kΩ function key on the 5005B front panel. Verify that the displays reads OPEN .
2. Sequentially connect the Timing Pod START/ST/SP (green), STOP/QUAL (red), and CLOCK (yellow) leads to the Data Probe tip. Verify that the display reads approximately 100 kΩ for each lead.
3. Connect the Timing Pod ground (black) lead to the Data Probe tip. Verify that the display reads zero ohms.

3-37. ERROR MESSAGES

3-38. Failures during the power-up self-check (and some modes of normal and remote operation) result in an error condition, detected by the 5005B and identified by a specific numbered ERROR MESSAGE and audible beeps.

3-39. For all error conditions, the 5005B initially displays "Err15". This display is meant to alert the operator of the error condition and prompt the request of the specific error number via the HP-IB. *If any error message is displayed, the operator should refer to Error Conditions, paragraph 3-94.*

3-40. CONDITIONAL DISPLAYS

3-41. Under certain circumstances, the 5005B will respond with a unique display representative of a special condition. The possible conditional displays and the corresponding meanings are listed in *Table 3-1* below.

Table 3-1. Conditional Displays

Function Mode	Display	Meaning
Signature Analysis NORM QUAL	- - - -	No measurement taken.
kHz	O F L O	Measurement overflow, input frequency ≥ 100 MHz.
TOTLZ	O F L O	Measurement overflow, events totalized > 99,999 counts.
ms	O F L O	Measurement overflow, time interval > 99,999 ms.
Vp+, Vp-	O L	Voltage peak ≥ 12.5 volts.
Vp+, Vp-	-O L	Voltage peak ≤ -12.5 volts.
⚠ DCV	O L -O L	Voltage ≥ 260 volts. Voltage ≤ -260 volts.
⚠ ΔV	O L -O L	Voltage of one reference point ≥ 260 volts. Voltage of one reference point ≤ -260 volts.
kΩ	O L -O L O L -O L O P E N	Drastic overload: ≈ 20 volts or greater. Positive voltage source >2 volts connected. Negative voltage source connected. Open circuit.
All	ErrXX	Internal error with identifying number.

3-42. GENERAL OPERATION INFORMATION

3-43. Recommended Operator Procedure

3-44. The 5005B performs analog type measurements (DCV, ΔV, Vp+, Vp-, and kΩ) and digital type measurements (SA NORM, SA QUAL, kHz, TOTLZ, and ms). For all digital measurement modes, the 5005B interprets input signal levels according to the settings of the POLARITY and THRESHOLD keys. That is, the active trigger edge (or state) for each of the Timing Pod inputs is

selectable with POLARITY keys. The logic family (TTL, ECL, or 5V CMOS) and the actual trigger threshold values within that family are selectable for the Data Probe and Timing Pod with the THRESHOLD keys. For any selected function, lighted LED indicators within the front panel POLARITY and THRESHOLD sections identify the active logic level and trigger threshold functions. The power-up state for POLARITY keys will be "rising edge". The power-up state for THRESHOLD keys will be TTL logic levels. To change from the power-up state to any other value or level, refer to paragraph 3-46.

3-45. The recommended sequence for setting-up and making a measurement with the 5005B is given below.

1. Set the 5005B LINE switch to ON. The 5005B should perform a power-up self-check, then preset to the NORM Signature mode.
2. Select the desired mode of operation by pressing the labeled FUNCTION key. The FUNCTION key indicator LED should light.
3. Select the desired POLARITY edges or level for the active CLOCK, START, STOP, and QUAL Timing Pod inputs.
4. Select the desired THRESHOLD logic family (TTL, ECL, or 5V CMOS) for the active DATA (Probe), CLOCK (Timing Pod), and ST/SP/QUAL (Timing Pod) inputs.
5. If necessary, reprogram the actual THRESHOLD levels for the *active* DATA (Probe), CLOCK (Timing Pod), and ST/SP/QUAL (Timing Pod) inputs, to desired nonstandard levels. Notice that the UNCAL LED indicator lights whenever a nonstandard THRESHOLD level is programmed.
6. Connect the Timing Pod leads and/or the Data Probe to the appropriate input signals.

3-46. Selecting Input POLARITY

3-47. The following paragraphs describe the procedure for selecting the POLARITY edges (or state) for the Timing Pod inputs. *Table 3-2* illustrates the POLARITY keys which are active for each digital measurement.

3-48. All four POLARITY keys, CLOCK, START, STOP, and QUAL, operate in a simple toggle fashion. Each keypress toggles the polarity to the complementary state. The lighted LED indicator identifies the active state.

1. To change the POLARITY edges for the CLOCK, START, or STOP Timing Pod inputs, press the corresponding labeled key. The indicator LED above the key identifies the active edge.
2. To change the POLARITY level for the QUAL Timing Pod input, press the QUAL key. The indicator LED above the key identifies the active level as follows: the left QUAL LED indicates a "HIGH" logic level, and the right QUAL LED indicates a "LOW" logic level.

Table 3-2. POLARITY Keys Active in Each Function

	POLARITY			
FUNCTION	CLOCK	START	STOP	QUAL
NORM	*	*	*	
QUAL	*	*	*	*
TOTLZ		*	*	
ms		*	*	

3-49. Selecting Standard Input Logic Family THRESHOLDS

3-50. The following paragraphs describe the procedure for selecting the input logic family with standard THRESHOLD levels for the Data Probe and Timing Pod inputs. *Table 3-3* illustrates which THRESHOLD keys are active for each function.

Table 3-3. THRESHOLD Keys Active in Each Function

	THRESHOLDS		
FUNCTION	DATA	CLOCK	ST/SP/QUAL
NORM	*	*	*
QUAL	*	*	*
kHz	*		
TOTLZ	*		*
ms			*

3-51. The 5005B is pre-programmed to trigger on the standard logic thresholds within the selected logic family (TTL, ECL, 5V CMOS). The 5005B automatically powers-up with the DATA (Probe), CLOCK (Timing Pod), and ST/SP/QUAL (Timing Pod) inputs set to standard TTL thresholds. The logic family for any input can be changed by repeatedly pressing the labeled input key until the desired TTL, ECL, or CMOS LED indicator is lighted. Pressing the key successively will cycle through all three standard logic family thresholds in a scrolling fashion, eventually returning to the starting point. The pre-programmed standard values for each logic family are given in *Table 3-4*. Notice that both a logic High and Low value for each logic family are programmed for the DATA (Probe), while only a logic family mean (midpoint) is required for the CLOCK and ST/SP/QUAL inputs.

1. To change the DATA (Probe) logic family THRESHOLD, press the labeled DATA key three times in sucession. The first press displays the TTL High THRESHOLD value (2.00H). The second press displays the TTL Low THRESHOLD value (0.80L). The third press changes the DATA threshold levels to the next logic family (ECL), and displays the High THRESHOLD value (-1.10H). Subsequent presses of the DATA key will recall and display the current High and Low THRESHOLD values, respectively, then change to the next logic family (5V CMOS).

   The currently active logic THRESHOLD values for the DATA (Probe) can be reviewed at any time by pressing the DATA key once for the High level, and once more for the Low level. If no keypresses are made for approximately two seconds, the display will return to the designated operating function.

2. To change the CLOCK or ST/SP/QUAL logic family THRESHOLD, press the labeled key twice. The first press displays the TTL THRESHOLD value (1.40). The second press changes the THRESHOLD to the next logic family (ECL), and displays the value (-1.30). Subsequent presses of the labeled key will recall and display the current THRESHOLD value, then change to the next logic family (5V CMOS).

   The currently active logic THRESHOLD values for the CLOCK and ST/SP/QUAL inputs can be reviewed at any time by pressing the respective key. If no keypresses are made for approximately two seconds, the display will return to the designated operating function.

Table 3-4. Standard Logic Family THRESHOLD Levels

	DATA	CLOCK	ST/SP/QUAL
TTL	2.00H 0.80L	1.40	1.40
ECL	-1.10H -1.50H	-1.30	-1.30
5V CMOS	3.50H 1.50L	2.50	2.50

3-52. Selecting Non-Standard Input Logic Family THRESHOLDS

3-53. The 5005B is pre-programmed to trigger on the standard logic thresholds within the selected logic family (TTL, ECL, 5V CMOS). The actual THRESHOLD values, however, may be changed to any desired level between ±12.50 volts, in 50 mV steps.

3-54. To change a THRESHOLD value, successively press the desired input key until the level to be changed is displayed. While the value is displayed, *immediately* press the NOISE MRG ADJUST up-arrow or down-arrow. The displayed value will slew up or down, respectively. Release the up/down-arrow key when the desired THRESHOLD value is displayed.

NOTE

Whenever any THRESHOLD level other than a standard value shown in *Table 3-4* is programmed, the "UNCAL" LED indicator will be lighted.

3-55. In general, a single press of an NOISE MRG ADJUST key will cause a 50mV step change in the displayed value. Holding the key "in" will cause a repeated stepping of the value at an increased speed. As an operator convenience, the 5005B pauses momentarily at the "standard" preset levels, while stepping through the THRESHOLD range. The adjustment range is ±12.50 volts for all THRESHOLDS. If no additional keypresses are made for approximately two seconds, the display will return to the designated operating function.

3-56. MODES OF OPERATION

3-57. The following paragraphs describe the modes of operation for the 5005B Signature Multimeter.

NOTE

Each measurement function of the 5005B is selected by pressing the corresponding labeled function key. Within each function, the *active* POLARITY and THRESHOLD keys will have annunciator LEDs lighted.

3-58. Signature Analysis Measurements/NORM (SIGNATURE/NORM)

3-59. The NORM Signature Analysis (SA) mode employs a unique data compression technique that reduces any long, complex data stream pattern on a logic node to a four-digit "signature". The operator supplies the Start and Stop signals to identify the data stream, and a Clock signal to control the sample rate of the probe input. An illustration of the timing involved in a Signature Analysis measurement window can be seen in *Figure 3-4.*

3-60. The 5005B makes Signature Analysis (SA) measurements on TTL, ECL, and 5V CMOS logic families. The trigger thresholds for the inputs are selectable from the standard preset values of the three logic families, or adjustable between -12.50V and +12.50V (in 50mV steps). The selected value for the ST/SP/QUAL THRESHOLD applies to both the Start and Stop signals, via the START/ST/SP and STOP/QUAL Timing Pod inputs. The slope for the Clock, Start, and Stop inputs is selectable using the POLARITY keys. The Start signal is applied to the START/ST/SP (green) Timing Pod lead. The Stop signal is applied to the STOP/QUAL (red) Timing Pod lead. The Clock signal is applied to the CLOCK (yellow) Timing Pod lead, and the measurement is made through the Data Probe.

3-61. During SA measurements, the GATE LED indicator will flash if there is an active Clock input. The Data Probe tip LED acts as a logic state indicator, lighting "brightly" for a logic high state, "dimly" for a three-state, and "off" for a logic low state. The Data Probe tip LED will "flash" to indicate activity at the node, however the flash duration is controlled by a pulse-stretching circuit and does not reflect the frequency of the input. The UNSTABLE LED will flash if there is a difference between two or more successive signatures. The maximum input clock rate for Signature Analysis modes is 25 MHz.

3-62. Signature Analysis Measurements/QUAL (SIGNATURE/QUAL)

3-63. The QUAL Signature Analysis mode is similar to the NORM mode, but with the following enhancement. In this mode, the STOP/QUAL input on the Timing Pod is sensed as a "data qualifier". Conceptually, the qualifier can be thought of as an "enable" signal. By controlling the logic state of this input, the operator can effectively window the signature measurement within a specific stream of data. Refer to *Figure 3-4*. The trigger thresholds for the inputs are selectable from the standard preset values of the three logic families (TTL, ECL, 5V CMOS), or adjustable between -12.5V and +12.5V (in 50mV steps). The selected value for the ST/SP/QUAL THRESHOLD applies to the Start, Stop, and Qualify signals, via the START/ST/SP and STOP/QUAL Timing Pod inputs. The slope for CLOCK, START, STOP and QUAL, is selectable using the POLARITY keys. When in the QUAL Signature mode, the red Timing Pod lead is the QUAL (qualifier) input, and the green Timing Pod lead is both the START *and* STOP input. The measurement is made through the Data Probe.

3-64. The operation of the GATE, UNSTABLE, and Data Probe tip LEDs during SA QUAL mode is the same as in SA NORM (see paragraph 3-61).

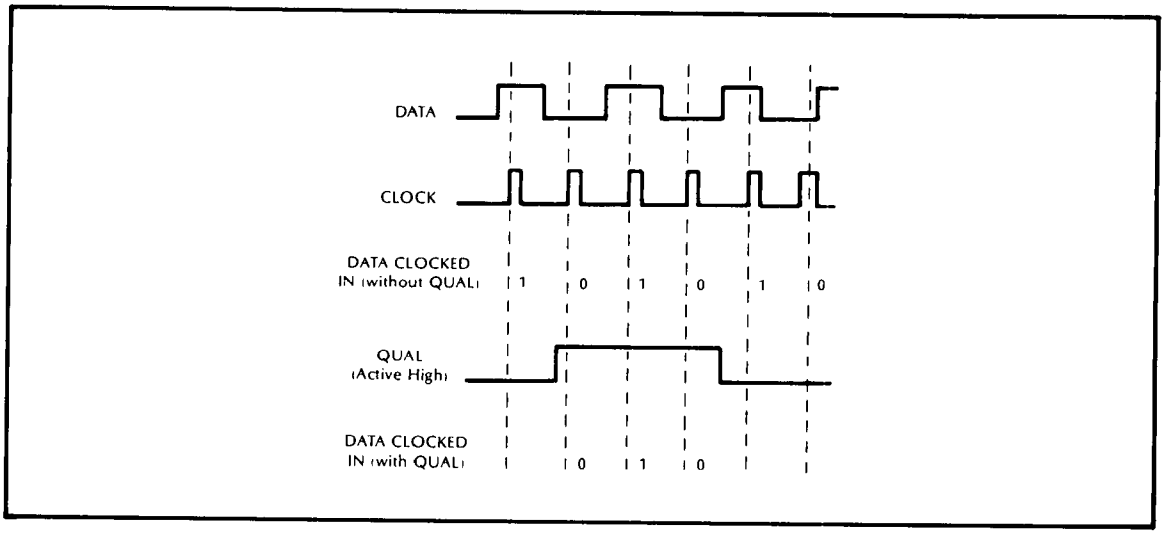


Figure 3-4. Signature Analysis Measurement Timing

3-65. Frequency Measurements (kHz)

3-66. The 5005B makes frequency measurements on input signals within the range of 0 to 50 MHz. The input signal is received through the Data Probe, with the trigger thresholds (logic high and low) determined by the values set by the THRESHOLD DATA key. Standard logic high and low thresholds are preset for each logic family (TTL, ECL, 5V CMOS). The actual thresholds can be reset, using the NOISE MRG ADJUST keys, to any value between -12.5V and +12.5V (in 50 mV steps). The input frequency is counted directly, with no prescaling techniques applied. Measurements are made in one of four ranges, 100 kHz, 1 MHz, 10 MHz, or 50 MHz, autoranged. The minimum pulse width is 10 ns. An input frequency greater than 100 MHz may result in a conditional display of "OFLO" (measurement overflow). The display multiplier/units value assigned is *always* assumed to be "kHz". The frequency mode GATE time is internally fixed at one second. This provides a resolution of 1 Hz up to 100 kHz, at which point the resolution becomes 1 LSD (least significant digit) for a five digit display. The accuracy is ±0.01% of the reading ±1 count.

3-67. Totalize Measurements (TOTLZ)

3-68. The Totalize mode of the 5005B counts the number of pulses or events occurring at the Data Probe, for a period of time specified by the Timing Pod START/ST/SP (green) and STOP/QUAL (red) inputs. The CLOCK input is not used. The trigger thresholds for the inputs are selectable from the standard preset values of the three logic families (TTL, ECL, 5V CMOS), or adjustable between -12.5V and +12.5V (in 50 mV steps). The selected value for the ST/SP/QUAL THRESHOLD applies to both START/ST/SP and STOP/QUAL Timing Pod inputs. The slope is selectable for both START/ST/SP and STOP/QUAL inputs using the POLARITY START and STOP keys. The Totalize mode can accumulate 0 to 99,999 events at a maximum rate of 50 MHz. The minimum pulse width is 10 ns, and minimum pulse separation is 10 ns. An input of more than 99,999 events may result in a conditional display of "OFLO" (measurement overflow). *Figure 3-5a* illustrates the asynchronous input timing relationships for the START, STOP, and DATA Totalize inputs. To achieve a ±0 count accuracy, the START signal should occur at least 50 ns before the first count transition on the Data Probe input, and the STOP must follow the last counted pulse by at least 50 ns. *Figure 3-5* also illustrates the synchronous input timing relationships for the START, STOP, and DATA Totalize inputs.

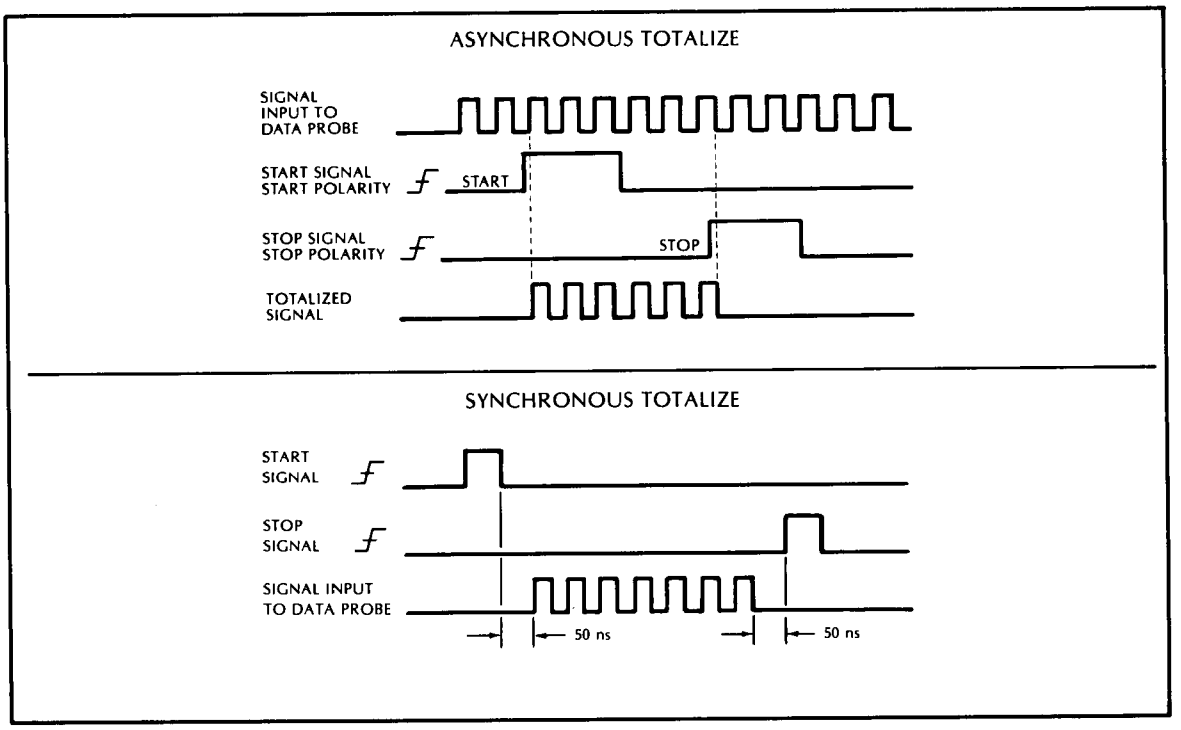


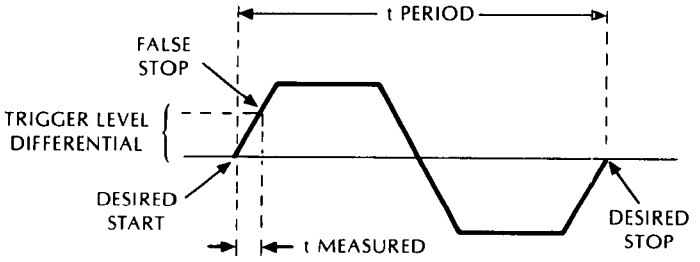
Figure 3-5. Totalize Measurement Timing

3-69. Time Interval Measurements (ms)

3-70. The Time Interval mode of the 5005B measures the length of time between a user defined START transition and STOP transition. A two source measurement uses the Timing Pod START/ST/SP (green) lead for the Start input and the STOP/QUAL (red) lead for the Stop input. For a single source measurement, the signal is applied to the Timing Pod START/ST/SP (green) input. The transition trigger threshold is selectable from the standard preset values of the three logic families (TTL, ECL, 5V CMOS), or adjustable between -12.5V and +12.5V (in 50 mV steps). The selected threshold value applies to both the Start and Stop inputs. The slope is selectable for both Start and Stop using the POLARITY START and STOP keys. The measurements are made in one of five ranges, 10 ms, 100 ms, 1 s, 10 s, or 100 s, autoranged. The minimum START/STOP pulse width is 20 ns. An input time interval of greater than 99,999 ms (100 s) may result in a conditional display of "OFLO" (measurement overflow). The display multiplier/units value assigned is *always* assumed to be "ms". The display range is 0 to 99,999 ms (milliseconds) with an accuracy of ±0.01% of the reading ±2 counts.

NOTE

The Start and Stop trigger thresholds are connected together internally, but differences do exist in the trigger circuitry. This results in a small differential between the Start and Stop trigger levels. This condition allows the possibility of unexpected measurements during the Time Interval mode. For example:



For Time Interval measurements, the expected result would be the period (t period) of the input sine wave. However, depending on the trigger level differential, an unexpected measurement (t measurement) may result.

3-71. Voltage Peak Measurements (Vp+, Vp-)

3-72. The 5005B measures positive (Vp+) and negative (Vp-) dc voltage peaks. The measurement range is 0 to 12.0V for positive peaks, and 0 to -12.0V for negative peaks. A peak input level more positive than 12.5V or more negative than -12.5V may result in a conditional (overload) display of "OL" or "-OL", respectively. The maximum time allowed between consecutive peaks is 50 ms (rate ≤20 Hz), with a minimum peak duration of ≥10 ns. The 3½ digit display provides resolution to 50 mV, with accuracy of ±2% of reading ±5% of p-p signal ±100 mV. The voltage peak measurement is made through the Data Probe. The Data Probe ground lead should be connected to the common ground of the source to be measured. The GATE and Data Probe tip LED indicators are not active in these modes. The operator should disregard any activity by the GATE and Data Probe tip LEDs.

⚠ 3-73. DC Voltage Measurements (DCV)

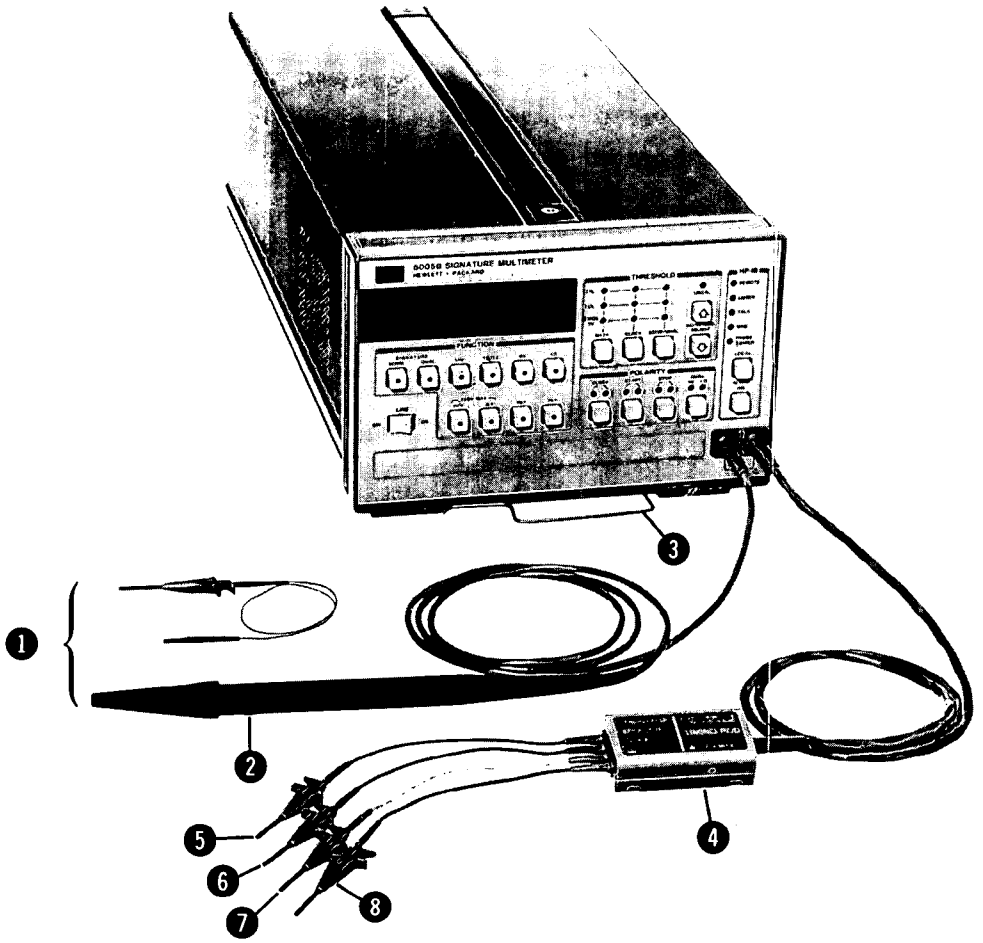
3-74. The 5005B measures dc volts (DCV) between plus 250V and minus 250V, referenced to earth ground. The digital voltmeter has two operating ranges, ±25V, and ±250V, autoranged, with polarity autoselected. An input level more positive than 260V or more negative than -260V may result in a conditional (overload) display of "OL" or "-OL", respectively. The 4½ digit display provides a resolution of 1 mV up to 25V, 10 mV from 25 to 100V, and 100 mV from 100 to 250V. Accuracy is ±0.1% ±2 mV (up to 25V), and ±0.25% ±20 mV (from 25 to 250V). The dc voltage measurements are made through the Data Probe. The Data Probe (or Timing Pod) ground lead should be connected to the earth or common ground of the source to be measured.

⚠ 3-75. Differential Voltage Measurements (ΔV)

3-76. The 5005B measures differential voltages between plus 250V and minus 250V (maximum differential 500V), referenced to an operator selected level. A reference level or a differential measurement more positive than 260V or more negative than -260V may result in a conditional (overload) display of "OL" or "-OL", respectively. The reference level is established by connecting the Data Probe tip to the desired level, and then pressing the ΔV function key (or the Data Probe switch). After approximately three seconds, the display will return with the programmed reference level, ≈0.000. All subsequent dc voltage measurements will automatically be compared to the reference level, and the difference voltage will be displayed. The 4½ digit display provides a resolution of 1mV (if both voltages are less than 25V), 10 mV (if the difference is between 25 and 100V), and 100 mV (if the difference is between 100 and 250V). Accuracy is ±0.1% ±2 mV (if both voltages are less than 25V), and ±0.25% (if either voltage is more than 25V). The differential voltage measurements are made through the Data Probe. *In this mode, the Data Probe ground lead (if used) must be at earth potential.*

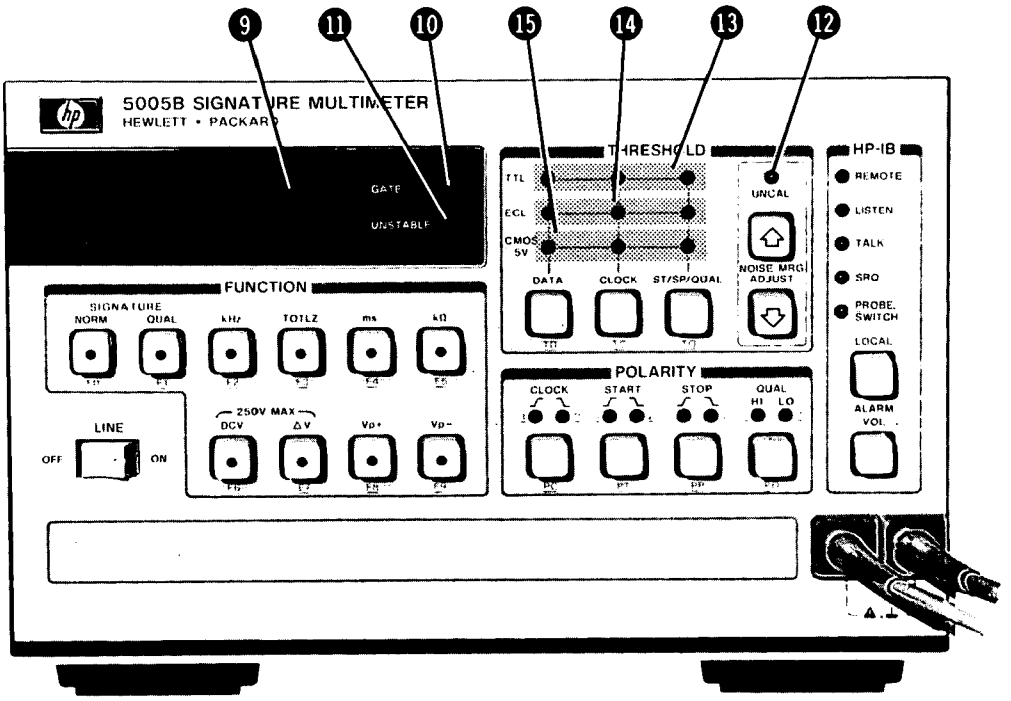
3-77. Resistance Measurements (kΩ)

3-78. The 5005B measures dc resistance from 0 to 10 MΩ. Measurements are made in one of five ranges, 30 kΩ, 300 kΩ, 1 MΩ, 3 MΩ, or 10 MΩ, autoranged. The display multiplier/units value assigned is *always* assumed to be "kΩ". Additional range, accuracy, and resolution information is provided in *Table 1-1, Specifications. Resistance measurements are made through the Data Probe, referenced to the Data Probe (or Timing Pod) ground leads. Be aware that the Timing Pod and Data Probe ground leads are connected internally to earth ground, and that resistance measurements should never be attempted on circuits with power applied. The 5005B provides internal protection circuits which sense dc voltage at the Data Probe tip. A dc source greater than plus 2 volts or minus volts connected to the Data Probe tip will automatically cause the probe to be "isolated" from the ohmmeter circuitry, via a relay, and may result in a conditional (overload) display of "OL" and "≅OL", respectively. An additional display of "OL-OL" (drastic overload) is possible if the protection circuitry senses* ±20 volts or more.



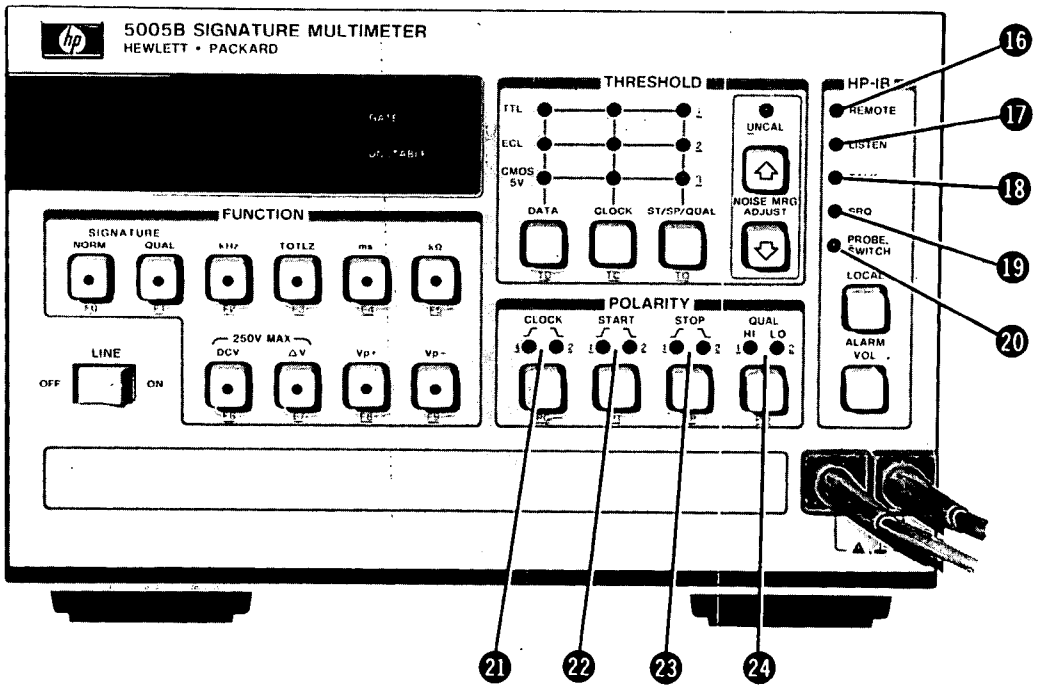
1 DATA PROBE, PROTECTIVE COVER, and GND LEAD	Point of entry for data or voltage for all function modes except Time Interval. For digital measurement modes SA Norm, SA Qual, kHz, and TOTLZ, the lamp within the data probe tip indicates the logic state of the input data: ON BRIGHT=High, ON DIM= Three-state, Off=Low, FLASHING=Activity. Note the removable ground connector wire (internally connected to earth ground) and the cap cover for the Data Probe tip.
2 DATA PROBE SWITCH	Used as an operator interactive prompt/response signal during remote operation. In local, can be used to set reference level during delta voltage (ΔV) measurements.
3 DATA PROBE POD HOLDER	Removable wire holder, used to cradle the Data Probe and Timing Pod when not in use.
4 TIMING POD	Supplies the three timing inputs, (START/ST/SP, STOP/QUAL, CLOCK, and Ground ⊥) from the Unit Under Test to the 5005B Signature Multimeter.
5 START/ST/SP	Point of entry for START signal in NORM or QUAL SA and Time Interval, and for both START and STOP signals in QUAL SA.
6 STOP/QUAL	Point of entry for STOP signal in NORM SA and Time Interval and for the QUAL signal in QUAL SA.
7 CLOCK	Point of entry for CLOCK signal during NORM and QUAL SA.
8 Ground ⊥	Common ground lead for all function modes. Note that this input is internally connected to earth ground.

Figure 3-6. Signature Multimeter, Data Probe and Timing Pod Features



9 DISPLAY	Contains the five seven-segment LED displays, and the preceding minus sign.
10 GATE LED	Flashing of GATE LED indicates 5005B is being gated.
11 UNSTABLE LED	Indicates an unstable signature reading.
12 UNCAL LED	Indicates that one or more of currently used input threshold levels is adjusted to a non-standard value.
13 TTL LEDs	Indicates the respective thresholds are set to test TTL logic. The TTL LED will be lighted even if the thresholds have been modified by the user. The UNCAL LED will light to indicate this condition.
14 ECL LEDs	Indicates the respective thresholds are set to test ECL logic. The ECL LED will be lighted even if the thresholds have been modified by the user. The UNCAL LED will light to indicate this condition.
15 5V CMOS LEDs	Indicates the respective thresholds are set to test 5V CMOS logic. The 5V CMOS LED will be lighted even if the thresholds have been modified by the user. The UNCAL LED will light to indicate this condition.

Figure 3-7. Front Panel Indicators



16 REMOTE — HP-IB status indicator lights when the 5005B is under remote control.

17 LISTEN — HP-IB status indicator lights when the 5005B is addressed to listen.

18 TALK — HP-IB status indicator lights when the 5005B is addressed to talk.

19 SRQ — HP-IB status indicator lights when the 5005B has requested service from the controller. SRQ line can be set by the 5005B in response to conditions defined by the Service Request Mask, provided the Service Request Mask has been set.

20 PROBE SWITCH — Probe switch status indicator. ON or flashing when the probe switch is enabled. Flashing indicates the 5005B is ready for a switch press, ON indicates the switch has been pressed.

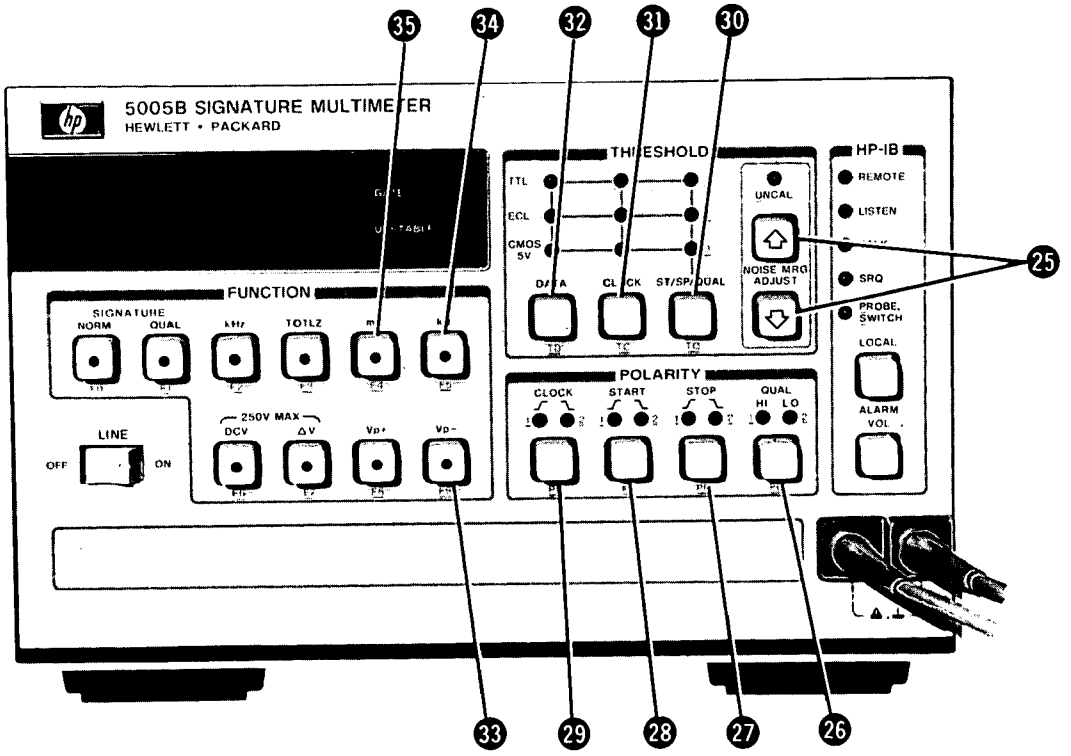
21 CLOCK — LED indicators for the status of the CLOCK polarity. Current active slope setting will be lighted.

22 START — LED indicators for the status of the START polarity. Current active slope setting will be lighted.

23 STOP — LED indicators for the status of the STOP polarity. Current active slope setting will be lighted.

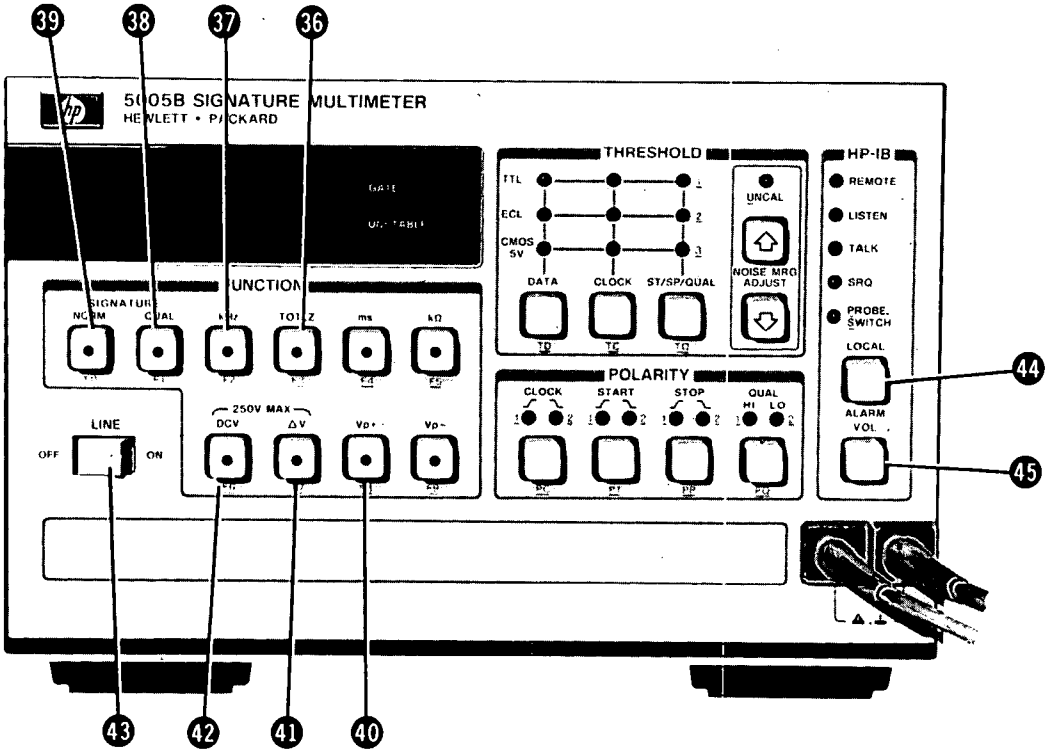
24 QUAL — LED indicators for the status of the QUAL polarity. Current active level setting will be lighted.

Figure 3-7. Front Panel Indicators (Cont.)



25	**NOISE MRG ADJUST**	Voltage threshold adjustment by single steps (or continuously if pressed and held) up or down in increments of 50 mV. Threshold adjustment pushbuttons can be used to check noise margins in the tested logic circuit.
26	**QUAL**	Selects whether the signature analysis is enabled by high or low level of the qualifying signal.
27	**STOP**	These three pushbuttons select either the positive-going or negative-going transition of the input signals to be used for timing of the measurements.
28	**START**	
29	**CLOCK**	
30	**ST/SP/QUAL**	This switch programs the ST/SP/QUAL inputs to operate with TTL, ECL, or 5V CMOS logic families.
31	**CLOCK**	This pushbutton programs the CLOCK input to operate with TTL, ECL, or 5V CMOS logic families.
32	**DATA**	This pushbutton programs the DATA input to operate with TTL, ECL, or 5V CMOS logic families.
33	**Vp-**	This pushbutton activates the negative peak voltage measurement.
34	**kΩ**	This pushbutton activates the resistance measurement. The measured resistance must be placed between the Data Probe tip and the Pod or Data Probe ground.
35	**ms**	The ms pushbutton activates the time interval measurements between the START and STOP signals at the Timing Pod leads.

Figure 3-8. Front Panel Controls



36 TOTLZ — This pushbutton activates the 5005B for counting the number of pulses at the input to the Data Probe occurring between the START and STOP pulses at the input to the Timing Pod.

37 kHz — The kHz pushbutton activates the 5005B for frequency measurements.

38 QUAL — The QUAL pushbutton activates the 5005B for signature analysis in the qualified mode. The CLOCK, START, STOP edges, and QUAL level as well as the logic thresholds are programmable in this mode.

39 NORM — The NORM pushbutton activates the 5005B for signature analysis in the normal mode. The CLOCK, START, and STOP trigger edges as well as the logic thresholds are programmable in this mode.

40 Vp+ — This pushbutton activates the positive peak voltage measurement.

41 ΔV — The delta volt pushbutton activates the 5005B to measure voltage levels at the Data Probe referenced to the voltage at the Data Probe at the time the ΔV pushbutton was pressed.

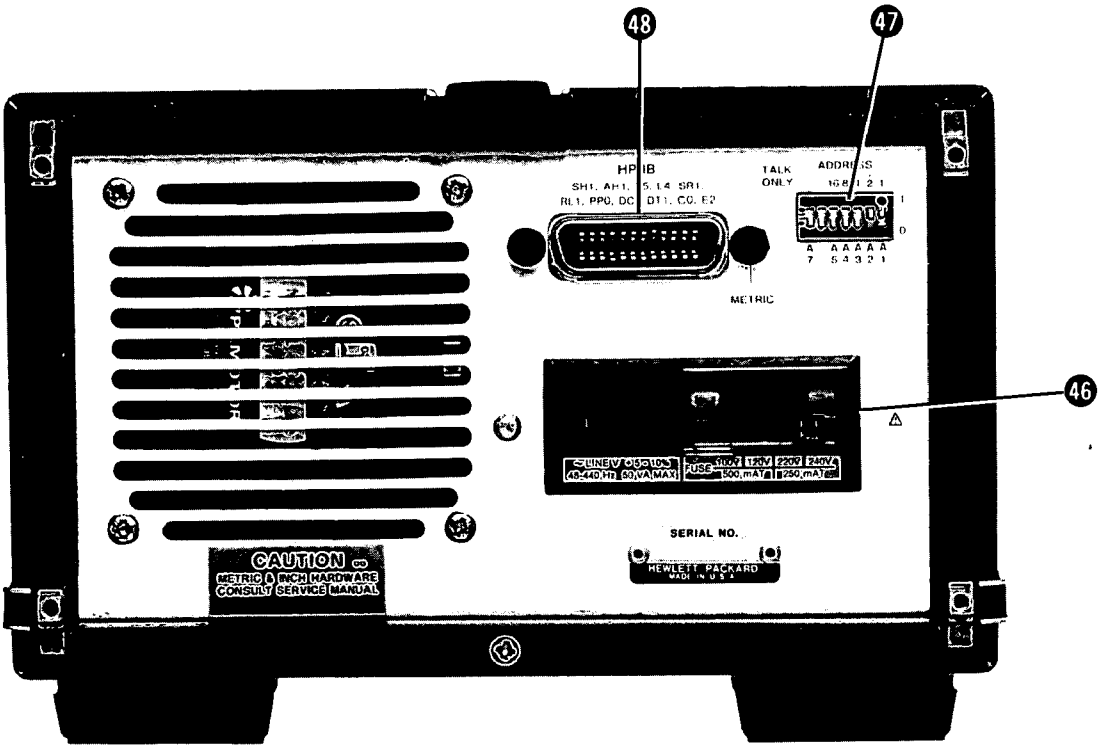
42 DCV — The DCV pushbutton activates the 5005B to measure the voltage at the Data Probe tip referenced to ground.

43 LINE OFF-ON — This is the main line switch for power to the 5005B.

44 LOCAL — This pushbutton places the 5005B back to "Local" operation when pressed while in REMOTE (unless the Local Lockout command has been issued).

45 ALARM VOL — This pushbutton operates in a toggle fashion, setting the volume of the alarm (beep) at either a low or high level. This key is not programmable.

Figure 3-8. Front Panel Controls (Cont.)



46 The AC power input module permits operation with 100, 120, 220, or 240 volts ac. The number visible in the window indicates nominal line voltage to which instrument must be connected (see *Figure 2-1*). Protective grounding conductor connects to the instrument through this module.

47 HP-IB address switches, contains switches A1 through A5. A6 is not used, A7 sets 5005B to TALK-ONLY or ADDRESSABLE modes.

48 HP-IB Interface Connector for remote operation via the HP-IB.

Figure 3-9. Rear Panel Features

Table 3-5. Operator's Check

OPERATOR'S CHECK PROCEDURE

NOTE

Before switching on the instrument, ensure that the voltage selector is set to the correct position, the correct fuse is installed, and the safety precautions, as described in Section II, paragraph 2-5 through 2-11, are observed.

STEP	PROCEDURE	RESULTS
1.	Set 5005B LINE switch to ON.	When the instrument is first turned-on, the instrument performs a self-test, indicated by all front panel LEDs lighted for a few seconds. The GATE and UNSTABLE LEDs flash momentarily. After self-test, the 5005B should be in the NORM Signature Analysis mode, with TTL thresholds selected and all positive polarities indicated by the respective LEDs. (Refer to paragraph 3-32.)

NOTE

Successful completion of the power-up self-check verifies the proper operation of the majority of circuitry. The following steps verify additional circuitry, not tested during self-test.

If during power-up or normal operation, error message 15 is displayed, the 5005B could be defective. Refer to Paragraph 3-37, ERROR MESSAGES, in this section.

2.	Press kΩ (•)	kΩ (☼) pushbutton LED lights. 5005B displays OPEn.
3.	Connect Data Probe tip to the Pod START/ ST/SP (green), STOP/ QUAL (red) and CLOCK (yellow) leads sequentially.	5005B measures approximately 100kΩ for each lead.
4.	Connect Data Probe tip to the Pod ground (black) lead.	5005B measures 0±.002 (kΩ).
5.		If all test results are normal, the operator can have a high degree of confidence that the 5005B is operating correctly.

Table 3-6. NORM Signature Analysis Measurement

NORM SIGNATURE ANALYSIS MEASUREMENT PROCEDURE

NOTE

Correct (expected) signatures for the Device Under Test (DUT) must be known for proper use of the 5005B. Signatures will usually be listed in the troubleshooting section of the DUT manual.

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press NORM .	NORM pushbutton lights.
2.	Connect START/ST/SP, STOP/QUAL, CLOCK, and Pod ground (⊥) leads to specified Start, Stop, and Clock test points, respectively,of the DUT. (Refer to DUT manual.)	
3.	Set DATA , CLOCK , and ST/SP/QUAL edges as stated in DUT manual. (Refer to paragraph 3-46).	Specified edges toggle and LEDs light. GATE light indicates gating.
4.	Set CLOCK , START , and STOP to the Logic family indicated in DUT manual. (Refer to paragraph 3-49).	Corresponding LEDs light.

NOTE

If the DUT manual specifies a 5004A Signature Analyzer, select only the preset TTL THRESHOLD levels.

Table 3-6. NORM Signature Analysis Measurement (Continued)

NORM SIGNATURE ANALYSIS MEASUREMENT PROCEDURE (Continued)

STEP	PROCEDURE	RESULTS
5.	The set-up can be checked by probing V_{CC} fro an expected signature.	5005B displays V_{CC} signature.
6.	Connect Data Probe to the tested node of DUT.	5005B displays test signatures to be compared with those in DUT manual.

NOTE

The first two signatures displayed may be wrong, noticeable only when very slow gating is used. In this condition the UNSTABLE LED will light and the signatures should be ignored. When a signature, which is different from the preceeding signature is displayed, the UNSTABLE LED lights. The first correct signature (following an incorrect signature) will have the UNSTABLE LED lighted. Only at the second correct signature will the UNSTABLE LED turn off. The 5005B has to read at least two consecutive identical signatures before the UNSTABLE LED will turn off.

DISPLAYED SIGNATURE	INCORRECT	INCORRECT	CORRECT	CORRECT	CORRECT
UNSTABLE LED	ON	ON	ON	OFF	OFF

Table 3-7. QUAL Signature Analysis Measurement

QUAL SIGNATURE ANALYSIS MEASUREMENT PROCEDURE

NOTE

Correct (expected) signatures for the Device Under Test (DUT) must be known for proper use of the 5005B. Signatures will usually be listed in the troubleshooting section of the DUT manual.

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press QUAL .	QUAL pushbutton lights.
2.	Connect START/ST/SP STOP/QUAL, CLOCK, and Pod ground (⊥) leads to specified test points of the DUT. (Refer to DUT manual.)	
3.	Set CLOCK , START , STOP edges and QUAL HI LO level as in DUT manual. (Refer to paragraph 3-46).	Specified edges toggle and LEDs light. GATE light indicates gating.
4.	Set DATA , CLOCK , and ST/SP/QUAL to the Logic family indicated in DUT manual. (Refer to paragraph 3-49).	Corresponding LEDs light.
5.	The set-up can be checked by probing V_{CC} for an expected signature.	5005B displays V_{CC} signature.

Table 3-7. QUAL Signature Analysis Measurement (Continued)

QUAL SIGNATURE ANALYSIS MEASUREMENT PROCEDURE (Continued)

STEP	PROCEDURE	RESULTS
6.	Connect Data Probe to the tested node of DUT.	5005B displays test signatures to be compared with those in DUT manual.

NOTE

The first two signatures displayed may be wrong, noticeable only when very slow gating is used. In this condition, the UNSTABLE LED will light and the signatures should be ignored. When a signature, which is different from the preceeding signature is displayed, the UNSTABLE LED lights. The first correct signature (following an incorrect signature) will have the UNSTABLE LED lighted. Only at the second correct signature will the UNSTABLE LED turn off. The 5005B has to read at least two consecutive identical signatures before the UNSTABLE LED will turn off.

DISPLAYED SIGNATURE	INCORRECT	INCORRECT	CORRECT	CORRECT	CORRECT
UNSTABLE LED	ON	ON	ON	OFF	OFF

Table 3-8. Frequency Measurement

FREQUENCY MEASUREMENT PROCEDURE

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press kHz.	kHz pushbutton lights. Gate LED flashes at the fixed 1Hz gating rate.
2.	Set DATA to desired logic family. (Refer to paragraph 3-49).	Selected logic family LED lights.
3.	Ensure one of the ground (⊥) leads is connected to the DUT ground. For frequencies above 10MHz, the Data Probe ground (⊥) lead should be used.	

NOTE

The frequency measured gate time is fixed at one second as indicated by the flashing GATE LED at the right of the display.

4.	Place the Data Probe tip on the signal to be measured.	Display shows the measured frequency with the GATE LED flashing at the measurement rate.

Table 3-9. Totalize Measurement

TOTALIZE MEASUREMENT PROCEDURE

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press TOTLZ.	TOTLZ pushbutton lights.
2.	Set desired START and STOP edges. (Refer to paragraph 3-46).	Selected edges toggle and LEDs light.
3.	Set DATA and ST/SP/QUAL to desired logic family. (Refer to paragraph 3-49).	Selected logic family LEDs light.
4.	Connect the Pod START/ST/SP and STOP/QUAL leads to the START and STOP signals.	
5.	Connect the Pod ground (⊥) lead to the ground of the DUT.	GATE light indicates gating.
6.	Place the Data Probe tip on the signal to be totalized.	Display shows the number of pulses occurring during the time between the Start and Stop edges.

Table 3-10. Time Interval Measurement

TIME INTERVAL MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press ms .	ms pushbutton lights.
2.	Set desired START and STOP edges. (Refer to paragraph 3-46).	Selected edges toggle and LEDs light.
3.	Set ST/SP/QUAL to desired logic family. (Refer to paragraph 3-49).	Selected logic family LED lights.
4.	Connect the Pod ground (⊥) lead to the ground of the DUT.	GATE light indicates gating.
5.	Connect the Pod START/ST/SP and STOP/QUAL leads to the START and STOP signals to be measured.	Display shows the time interval between selected transitions of the START and STOP signals.

Table 3-11. Resistance Measurement

RESISTANCE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press kΩ .	kΩ pushbutton lights. If the Data Probe is not connected, the 5005B displays OPEN .

CAUTION

Before taking resistance measurements, ensure the tested circuit is not under power and is disconnected from the earth ground. This can normally be done by disconnecting the AC power cord.

2.	Connect Data Probe ground (⊥) lead on one side of resistance to be measured.	
3.	Place Data Probe tip on other side of resistance to be measured.	Display shows the measured resistance between the Data Probe tip and ground.

Table 3-12. Voltage Measurement

VOLTAGE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press DCV [•].	DCV [☼] pushbutton lights.
2.	Connect Data Probe or Pod ground (⊥) lead to the common ground point of source to be measured.	
3.	Place Data Probe tip on voltage point to be measured.	Display shows the measured voltage between the Data Probe and ground.

CAUTION

The Ground input of the DVM is attached to earth ground via the instrument chassis. Do not connect to any voltage other than earth ground.

Table 3-13. Difference Voltage Measurement

DIFFERENCE VOLTAGE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Connect Data Probe or Pod ground (⊥) lead to the common ground point of source to be measured.	
2.	Place Data Probe tip on circuit point to be used as a voltage reference point. Press and hold Δv ⊙ OR the Data Probe switch. Hold Data Probe on voltage reference until a numeric display (≈ 0.000) appears.	Δv ☼ pushbutton lights. 5005B displays zero voltage difference. This is the reference voltage for the following difference measurements.
3.	Place Data Probe tip on the circuit point whose voltage is to be measured.	Display shows the voltage difference between the currently probed circuit point and the previously defined reference (step 2) point.

Table 3-14. Peak Voltage Measurement

PEAK VOLTAGE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press Vp+ ⊙ or Vp− ⊙	Selected pushbutton lights.
2.	Connect Data Probe ground (⊥) lead to the ground of test. Leaving the Data Probe ground disconnected will result in inaccurate measurements.	

NOTE

Disregard blinking of GATE LED and Data Probe logic light.

3.	Place Data Probe tip on the circuit point at which peak plus or minus voltage is to be measured. Do not exceed (+) or (−) 12.0 Vdc.	Display shows the peak voltage value at the Data Probe.

3-79. REMOTE PROGRAMMING VIA THE HP-IB

3-80. Introduction

3-81. The 5005B Signature Multimeter is compatible with the Hewlett-Packard Interface Bus (HP-IB). Remote Programming is installed as standard equipment and allows the instrument to respond to remote control instructions and output measurement data via the HP-IB. At the simplest level, the 5005B can output data in the talk only mode to other devices such as a controller or printer. In more sophisticated systems, a computing or other type of controller can remotely program the 5005B to perform a specific type of measurement, trigger the measurement, and collect the results.

NOTE

HP-IB is Hewlett-Packard's implementation of IEEE Std. 488-1978, *Standard Digital Interface for Programming Instrumentation".*

3-82. The operator must be familiar with the selected controller (e.g., the 9825A/B, 9826A, 9830A, 9835/45A, or 85A), the HP-IB, and the manual operation and functional capabilities of the 5005B. The following HP manuals should provide useful background information:

Hewlett-Packard 85 Owner's Manual and Programming Guide (P/N 00085-90002)
Hewlett-Packard 85 I/O Programming Guide (P/N 00085-90142)
Hewlett-Packard 9825A Calculator Operating and Programming Manual (P/N 09825-9000)
Hewlett-Packard 9825A String Variable Programming (P/N 09825-90020)
Hewlett-Packard 9825A Calculator General I/O Programming (P/N 09825-90024)
Hewlett-Packard 9825A Calculator Extended I/O Programming(P/N 09825-90025)
Hewlett-Packard 9825B Manual Kit (P/N 09825-87901)
Hewlett-Packard 9826A BASIC Manual Set (P/N 09826-87902)
Hewlett-Packard 9835A Operating and Programming Guide (P/N 09835-90000)
Hewlett-Packard 9835A I/O ROM Programming Manual (P/N 09835-90060)
Hewlett-Packard 9845A Operating and Programming Guide (P/N 09845-90060)
Condensed Description of the Hewlett-Packard Interface Bus(P/N 59401-90030)
HP-IB Programming Hints For Selected Instruments (P/N 59300-90005)
HP-IB User Guide, 9830A (P/N 59300-90002)
Tutorial Description of the Hewlett-Packard Interface Bus (P/N 5952-0156)

3-83. BUS COMPATIBILITY

3-84. Interface Functions

3-85. The capability of a device connected to the bus is specified by its interface functions. These functions provide the means for a device to receive, process, and send messages over the bus. *Table 3-15* lists the 5005B interface functions using the terminology of the IEEE 488-1978 standard. These functions are also listed above the rear panel HP-IB connector, as follows:

SH1, AH1, T5, L4, SR1, RL1, PP0, DC1, DT1, C0, E2

3-86. The number following the interface function code indicates the particular capability of that function.

Table 3-15. HP-IB Interface Functions

INTERFACE FUNCTION SUBSET IDENTIFIER	INTERFACE FUNCTION DESCRIPTION
SH1	Complete source handshake capability.
AH1	Complete acceptor handshake capability.
T5	Talker (basic talker, serial poll, talk only mode, and unaddress if MLA capabilities).
L4	Listener (basic listener, no listen only, and unaddress if MTA capabilities).
SR1	Service request capability.
RL1	Complete remote/local capability.
PP0	No parallel poll capability.
DC1	Complete device clear capability.
DT1	Device trigger capability.
C0	No controller capability.
E2	Three-state bus drivers.

3-87. The 5005B operates (as listed in *Table 3-15*) as both a talker and listener. The 5005B output format is the same regardless of the mode (talk only/addressable).

a. TALK: The 5005B can be addressed to Talk by a controller or by the TALK ONLY switch. When addressed as a Talker, the 5005B will send data to other devices on the bus. This data is the result of the measurement or the next measurement, depending on the function selected. The TALK ONLY switch and the HP-IB address switches are located on the rear panel (see *Figure 3-10*).

NOTE

To remove the 5005B from the TALK ONLY mode, set the TALK ONLY switch A7 to "O" and cycle the line power.

b. LISTEN: When addressed as a Listener, the instrument can accept any number of commands from the controller via the bus. These commands are used to program the instrument operation.

c. SERVICE REQUEST (SRQ): SRQ can be sent active on the bus at the end of the measurement. The 5005B has the capability to request service asynchronously from the controller in charge of the bus. See "QM" command described in Service Request Mask, paragraph 3-131.

d. REMOTE/LOCAL: Normally, the 5005B is under front panel (local) control. To program the 5005B, it must be placed in Remote. Once in Remote, programmable functions cannot be affected by front panel control, except the LOCAL and ALARM VOL keys. The LOCAL key may be used to return the 5005B to local control. This key may be disabled with Local Lockout (LLO). In LLO, the bus command LOCAL must be sent to disable LLO.

e. PARALLEL POLL: The 5005B does not respond to a parallel poll.

f. DEVICE CLEAR: When a group or selected device clear is received, the 5005B clears the error (if present), resets *and initiates a new measurement*.

g. DEVICE TRIGGER: When a device trigger is received, the 5005B will make a new measurement and wait for data collection.

h. CONTROLLER: The 5005B cannot act as a controller.

i. DRIVERS: The 5005B has three-state output bus drivers. The output bus goes to the three-state whenever it is not in TALK.

3-88. BUS MESSAGES

3-89. Through bus messages, devices on the bus can exchange control and measurement information. There are twelve basic messages which can be sent over the interface. *Table 3-16* lists each bus message, giving a description, the 5005B response, and examples of various controllers' implementation of the messages. The following paragraphs provide a more detailed description of these messages.

3-90. Bus Message Response

a. REMOTE: The 5005B goes remote when it receives the REMOTE message on the HP-IB. All front panel controls except the LOCAL key are ignored. In REMOTE operation, the 5005B is programmed by the controller via messages sent over the bus. Until changed, the state of the 5005B remains as it was prior to receipt of the REMOTE message.

b. LOCAL: Returns the 5005B to front panel control. Otherwise, the state remains as it was prior to receipt of the LOCAL message.

NOTE

The 5005B does not respond to any messages other than REMOTE, STATUS, TRIGGER, CLEAR, and DATA messages when in LOCAL operation.

c. LOCAL LOCKOUT: Disables the 5005B LOCAL key. The 5005B remains in remote operation until a LOCAL message is received on the bus. The LOCAL LOCKOUT message can be used to maintain "absolute" programmatic control of the 5005B.

d. GO TO LOCAL AND CLEAR LOCAL LOCKOUT: Returns the 5005B to front panel control following a LOCAL LOCKOUT message. Otherwise, the state of the 5005B remains as it was prior to receipt of the GTLCLL message.

e. ABORT: Terminates any HP-IB activity and returns control to the system controller. Parameters remain as they were before the ABORT message. Any partially entered HP-IB data message is aborted.

f. CLEAR: Initiates a new measurement.

g. TRIGGER: The 5005B takes a measurement and waits for the controller to collect the data. Any other command will cancel the wait status. When the 5005B is group or single triggered, it will wait for data collection.

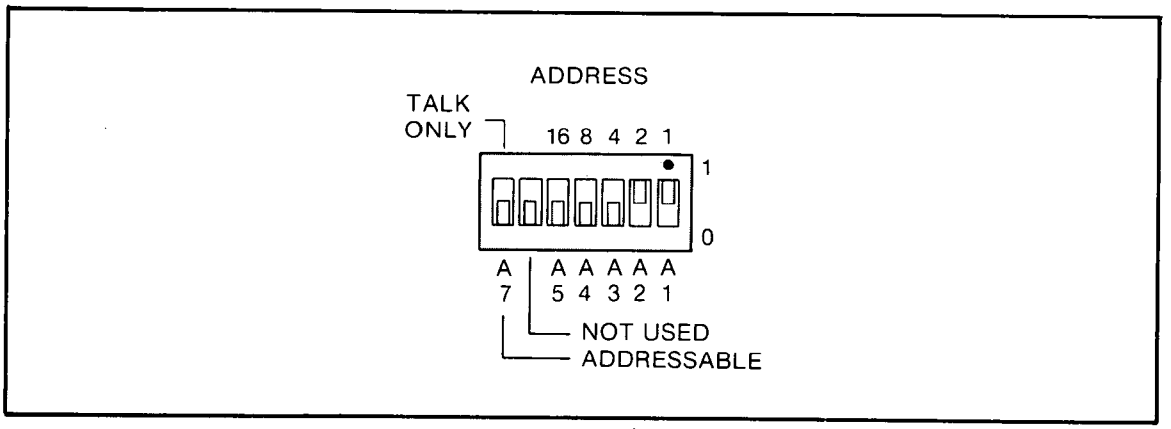


Figure 3-10. 5005B Address Switches

Table 3-16. Bus Messages

HP-IB MESSAGE	DESCRIPTION/RESPONSE	SAMPLE 9825A (address=03)	SAMPLE 85A (address=03)
DATA	A means to send commands to and receive measurement data from the 5005B.	wrt 703,"F1" red 703,A	OUTPUT 703;"F1" ENTER 703; A
TRIGGER	Starts a new measurement, if the 5005B is in remote, or local & listen.	trg 7	TRIGGER 7
	Starts a new measurement. If the 5005B is in local, the 5005B will go into remote.	trg 703	TRIGGER 703
CLEAR	Starts a new measurement.	clr 7 clr 703	CLEAR 7 CLEAR 703
REMOTE	Front panel function keys are disabled (except LOCAL and ALARM VOL). All settings remain unchanged unless modified by a data message.	rem 703	REMOTE 703
LOCAL	Returns the 5005B to local (front panel) control.	lcl 703	LOCAL 703
LOCAL LOCKOUT	Disables front panel keys; only controller can return 5005B to local.	llo 7	LOCAL LOCKOUT 7
GOTO LOCAL AND CLEAR LOCAL LOCKOUT	Returns all devices on the bus to local (front panel) control; local lockout cleared.	lcl 7	LOCAL 7
SERVICE REQUEST	5005B will request service from the controller after meeting the condition(s) set by the service request mask (command QM).	rds (703) (DEVICE STATUS)	A= SPOLL (703)
STATUS BYTE	Presents status information.	rds (703) (BUS STATUS)	A= SPOLL (703)
STATUS BIT	Not applicable		
PASS CONTROL	Not applicable		
ABORT	Terminates all bus communications; tells all devices to unlisten; listen LED will go out.	cli 7	ABORTIO 7

h. SERVICE REQUEST: When in remote operation, the 5005B can send a SERVICE REQUEST message (SRQ) to the controller under any or all of the following condition(s), as defined by the Service Request Mask. The Service Request Mask (QM command, see paragraph 3-131) must be set prior to the condition.

1. Data ready. A measurement has been completed and is available for collection.
2. Probe Switch pressed. The probe switch has been pressed to initiate a measurement.
3. Error. An error condition exists.

i. STATUS BYTE: The controller can read the 5005B STATUS BYTE at any time to check selected operating conditions. The assignment of the bits of the 5005B STATUS BYTE are shown in *Table 3-17.*

Table 3-17. 5005B Status Byte

D7	D6	D5	D4	D3	D2	D1	D0
0	SRQ FLAG	POWER ON OK	LOCAL	BUSY	ERROR	PROBE SWITCH PUSHED	DATA READY
128	64	32	16	8	4	2	1

A decimal number equivalent to the sum of the different status bits will be sent in response to the status request.

j. STATUS BIT: Not used.

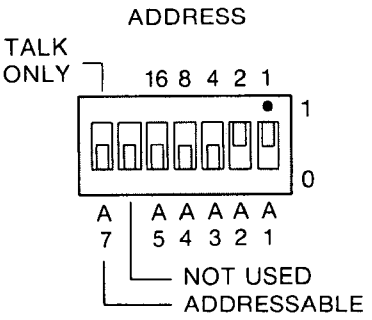
k. PASS CONTROL: Not used.

3-91. ADDRESS SELECTION

3-92. To use the 5005B in an HP-IB system, set the rear panel address switches to the desired address. The leftmost switch sets the 5005B to either the addressable or TALK ONLY mode. The addressable mode is used when the 5005B functions as a talker and listener. The TALK ONLY mode is employed when the 5005B is operating in an output only condition. In this mode, the 5005B will send data to a controller or other listeners when the probe switch is pressed.

3-93. The five rightmost switches, A5 through A1, set the TALK and LISTEN addresses of the 5005B when it is used in the addressable mode. *Table 3-18* shows all possible address settings and the corresponding ASCII codes for talk and listen. The 5005B is factory set to address 03 as shown in *Figure 3-10.*

Table 3-18. Address Selection



(Shown in addressable mode, and address 03)

NOTE

Select the decimal listen address from the table below and set the address switches to the corresponding positions.

ASCII CODE CHARACTER		ADDRESS SWITCHES					5-BIT DECIMAL CODE
LISTEN	TALK	A_5	A_4	A_3	A_2	A_1	
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
"	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
—	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
Ø	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21 ◄
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	\	1	1	1	0	0	28
=	]	1	1	1	0	1	29
>	~	1	1	1	1	0	30

Address "21" is preset controller address.

3-94. 5005B ERROR CONDITIONS

3-95. Failures during the power-up self-check (and some modes of normal and remote operation) result in an error condition, detected by the 5005B and identified by a specific numbered ERROR MESSAGE and audible beeps. The following paragraphs describe how to identify the specific error number and corresponding ERROR MESSAGE. The flowchart in *Figure 3-11* illustrates the sequence of operator steps.

3-96. For most error conditions, the 5005B initially displays "Err15". This display is meant to alert the operator of the error condition and prompt the request of the error number via the HP-IB.

3-97. When the 5005B detects an error condition, Err15 is displayed and the alarm will sound. If the Err15 occurs while in remote, pressing the LOCAL key or having the controller send "GO TO LOCAL" or the "DCL" command, will clear the "Err15" display. To access the error code, wait three seconds for the "Err15" to clear, then have the controller execute an error code recovery routine, as illustrated in *Figure 3-11*. After the controller sends the "SE" (Send Error) command, the 5005B returns a decimal representation of the individual error. After clearing an error condition, the front panel set-up must be re-established.

HP85A Error Code Recovery Routine

```
10 LOCAL 7
20 WAIT 3000
30 REMOTE 703
40 OUTPUT 703;"SE"
50 ENTER 703;A
60 DISP A
70 END
```

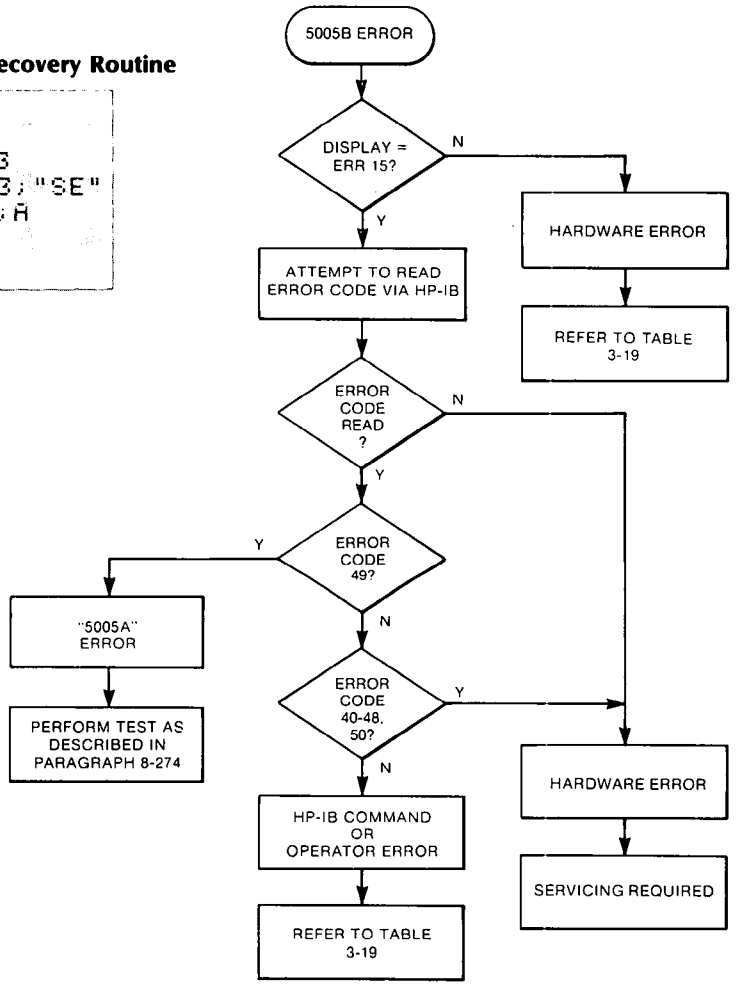


Figure 3-11. 5005B Error Message Flowchart

3-98. There are 19 ERROR MESSAGES applicable to the 5005B HP-IB Hardware, Operating Software, and Commands. They are assigned numbers between 40 and 88, as listed in *Table 3-19.* Errors 40 through 50 will require servicing to correct. Errors 81 through 88 are operator or controller errors which may be cleared (see paragraph 3-97) and re-attempted.

Table 3-19. HP-IB Error Codes

Hardware and Operating Software Related Errors	
Error 40	Function key LED error. Either none or more than one function key LED(s) on. Implies a 5005A* failure, Port C4 failure or 5005B in some diagnostic mode (e.g., display test).
Error 41	Attempt to push illegal key code (>18).
Error 42	Unrecognized character read from display; error found during ASCII conversion. Implies 5005A* failure or Port C4 failure.
Error 43	No response to key depression.
Error 44	Internal error during command interpretation; offset counter incorrect. Fatal error.
Error 45	Internal error. Parameter out of range. Fatal.
Error 46	Invalid interrupt on HP-IB interrupt line.
Error 47	Illegal key code read from keyboard IC (74C923).
Error 48	Display IC (7218) digit strobe error. Implies IC failure or Port C5 failure.
Error 49	ERXX read from 5005A display. (See paragraph 8-274 for procedure to identify errors 0-20.
Error 50	Two or more mutually exclusive polarity select leds, or two or more mutually exclusive threshold select leds found on during "SU" execution.
HP-IB Command and Operation Related Errors	
Error 81	Command string too long (over 250 characters).
Error 82	No match for HP-IB command. Implies illegal or incomplete HP-IB command.
Error 83	Illegal or missing numeric trailer in HP-IB command.
Error 84	Attempted selection of an edge select or threshold select not active in this function.
Error 85	HP-IB IC (8291) "Err" bit set. Implies no active listeners on the bus. Controller error.
Error 86	Illegal threshold voltage command format.
Error 87	Programmed threshold voltage out of range.
Error 88	Local Key pushed and some function other than delta volts selected after remote selection of delta volts. The delta volts reference is no longer valid, resulting in the possibility of erroneous data being sent to the controller.

* Error conditions caused by any 5005B circuitry other than the HP-IB assembly itself are considered "5005A" errors.

3-99. FRONT PANEL HP-IB STATUS LEDs

3-100. The four HP-IB status LEDs on the front panel indicate the status of the 5005B. The REMOTE LED lights to indicate that the 5005B is under remote control. The LISTEN LED lights to indicate that the 5005B is addressed to listen (receive commands). The TALK LED lights to indicate that the 5005B is addressed to talk (send data). The SRQ LED lights to indicate that a service request condition exists (as determined by a set service request mask bit).

3-101. When the 5005B returns from remote operation to the local mode, the REMOTE LED turns off. The TALK or LISTEN, SRQ, and PROBE SWITCH LEDs will remain in their current state. If the 5005B is unaddressed, the PROBE SWITCH and SRQ LEDs will remain in their current state. In the TALK ONLY mode, the TALK and PROBE SWITCH LEDs are always lighted.

3-102. In addition to the HP-IB status LEDs, the front panel PROBE SWITCH status LED indicates the present condition of the probe switch. When this LED is flashing, the probe switch is enabled and ready for a switch press. Pressing the probe switch initiates a measurement. The PROBE SWITCH LED goes from flashing to ON to indicate that the probe switch has been pressed. In many real time measurement environments, however, the flashing to ON (then back to flashing) lighting sequence may be too fast to see. After the PROBE SWITCH LED responds, the measurement information is ready for collection by the controller.

3-103. HP-IB COMMAND CODE SYNTAX DIAGRAMS

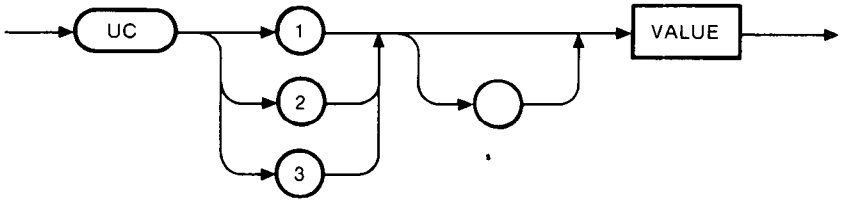
3-104. Statement syntax is represented pictorially throughout this section, to explain the format in which HP-IB programming commands should be sent to the instrument. All characters enclosed by a rounded envelope must be entered exactly as shown. Words enclosed by a rectangular box are names of items used in the statement and are described in the text following the diagram. Items contained within circles indicate required literals which must occur in the statement syntax exactly as shown.

NOTE

Spaces are not included in all instances where they may occur. Rather, they are included as (optional) additions to the command string in places where clarity is gained by their use.

3-105. Statement elements, connected by lines, can be followed in only one direction as indicated by the arrowhead at the end of the line. Any combination of statement elements that can be generated by following the lines in the proper direction is syntactically correct.

3-106. The syntax drawing example shown below illustrates the use of the uncalibrated Clock threshold setting command.



VALUE — The range of acceptable threshold values is −12.50 V to +12.50 V. The data must be sent in the following format:

± XX.XX

The "+" sign and the leading "0" are optional. The least significant digit must be either a "0" or a "5". For example, acceptable values are −11.75, 0.05, +03.60, 9.85. Unacceptable values are −13.60 (out of range), 0.6 (no LSB), +03.67 (LSB not 0 or 5), 9 . (no LSB).

3-107. By following the arrowheads on the lines, the acceptable command codes are:

UC1 (with some value)

UC2 (with some value)

UC3 (with some value)

3-108. The value description occurs in text following the diagram to indicate acceptable values for this parameter. Therefore, acceptable command strings are:

UC1-4.65

UC2-04.65

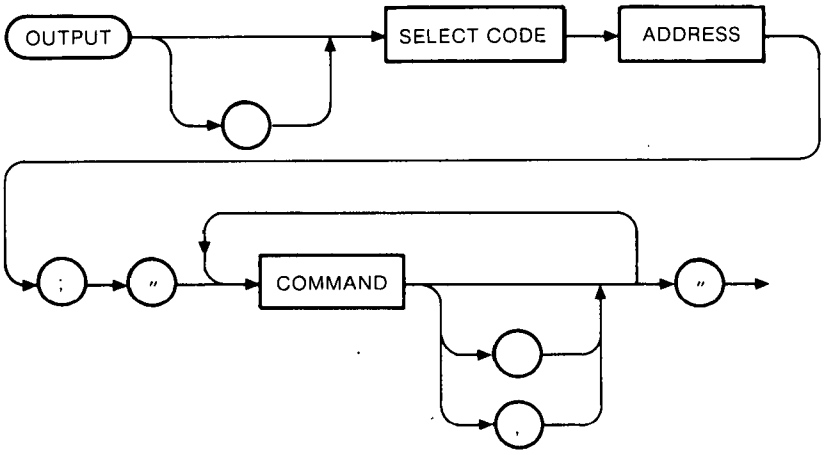
UC3 0.45

3-109. INPUT CODE FORMAT

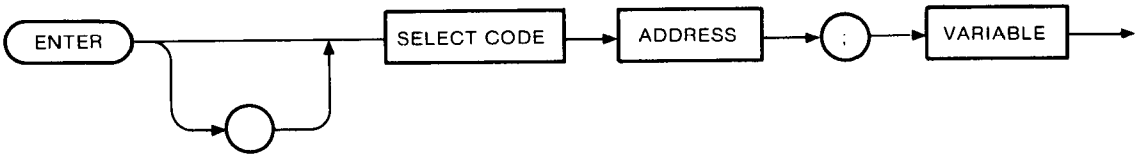
3-110. The 5005B will accept command strings in either upper or lower case. Spaces and commas between commands are ignored. Semicolons are interpreted as line terminators. In addition, parity bits will be ignored. Depending upon the controller, this can help to speed up programming. The following command statements will produce identical results:

OUTPUT 703; "F1AL2QM2PS1"

output 703; "f1al2qm2ps1"



SELECT CODE — SELECT CODE DIGIT FOR CONTROLLER (USUALLY 7)
ADDRESS — ADDRESS OF 5005B AS DETERMINED BY REAR PANEL ADDRESS SWITCHES
COMMAND — STRING OR SEQUENCE OF ASCII BYTES



SELECT CODE — SELECT CODE DIGIT FOR CONTROLLER (USUALLY 7)
ADDRESS — ADDRESS OF 5005B AS DETERMINED BY REAR PANEL ADDRESS SWITCHES
COMMAND — STRING OR SEQUENCE OF ASCII BYTES

VARIABLE — A NUMERIC OR STRING VARIABLE TO STORE THE READ INFORMATION

3-112. OUTPUT FORMAT

3-113. The 5005B HP-IB assembly microprocessor continuously reads the display data during a measurement and stores the most recent value. The 5005B can output this stored information to the HP-IB in the talk mode.

3-114. TALK ONLY MODE

3-115. To place the 5005B in the TALK ONLY mode, address switch A7 must be set to the TALK ONLY position, and the line power must be cycled. In this state, the front panel TALK status LED will be lighted and the PROBE SWITCH LED will flash. Each press of the Data Probe switch sends measurement data to the controller. The output data format for measurement information sent via the HP-IB is:

Signature	XXXX		CR	LF	
Frequency	XX.X.X.X.	E+3	CR	LF	
Totalize	XXXXX	E+0	CR	LF	
Time Interval	X.X.X.X.X.	E-3	CR	LF	
kΩ	XX.X.X.X	E+3	CR	LF	Open circuit: 9.9999 E19 CR LF
DCV	(-)XX.X.XX	E+0	CR	LF	
ΔV	(-)XX.X.XX	E+0	CR	LF	
VP+	(-) XX.XX	E+0	CR	LF	
Vp-	(-) XX.XX	E+0	CR	LF	

NOTE

The SIGNATURE (NORM and QUAL), Vp+, and Vp- function modes will output four digits as shown. All other modes output five digits. The position of the decimal point within the five digit output will vary, dependant upon the range autoselected by the 5005B (refer to *Table 1-1*, Specifications). The decimal point may be in any one of the positions indicated. In the FREQUENCY mode, for example, the output format appears as "XX.X.X.X.". This means that five digits and a decimal point will be output in one of the following formats:

XX.XXX
XXX.XX
XXXX.X
XXXXX.

3-116. All data overflow conditions yield 9.9999 E+09 CR LF. In an error condition, the response is "9E29".

3-117. MEASUREMENT TRIGGERING IN REMOTE

3-118. In remote, the 5005B operates in a free run status, with most modes self-armed and self-triggered. In general, programming and sending any function change causes the function to change and measurements to automatically commence. For all functions, the latest completed data is available after the 5005B completes the measurement. The following paragraphs describe specific measurement cycles for the various 5005B functions.

3-119. **F0, F1, F2, F3, and F4.** For NORM SA (F0), QUAL SA (F1), kHz (F2), TOTL (F3), and ms (F4), the 5005B continously monitors the gate light (GATE). When the gate light changes from "on" to "off", the data is read and stored until the controller collects the data or until the data is replaced during the next measurement cycle.

3-120. **F5, F6, F8, and F9.** For kΩ(F5), DCV (F6), Vp+ (F8) and Vp- (F9), the 5005B continously reads the display and stores the data for the controller to collect.

3-121. **F7.** For ΔV (F7), a reference voltage must first be established before difference voltage measurements can be taken. The recommended procedure for remote ΔV operation is as follows:

a. The controller sends the function command "F7" for ΔV. This causes the 5005B function to change to ΔV, and the front panel PROBE SWITCH LED to flash.

b. The controller should advise the operator of the proper reference node location, and place the 5005B in the "talk" mode.

c. The operator should locate the reference node with the Data Probe tip, and then press the Data Probe switch, which triggers the reference measurement. After approximately three seconds, the display should change from "----" to the "reference value" (≈0.000), and the PROBE SWITCH LED should go from flashing to on. The reference value is sent back so that the controller knows the reference is established. After the controller collects the data, the PROBE SWITCH LED again begins to flash. If the operator needs to know the reference voltage, place the Data Probe tip to "Gnd" and press the Data Probe switch. The first difference reading will be the same value as the reference voltage, but with the opposite sign.

d. The controller should advise the operator of the (next) test node. A press of the Data Probe switch will cause a difference voltage measurement and subsequent data collection.

e. If the controller needs a second or refreshed reference voltage or setup, the function command (F7) should be sent again. Repeat the procedure described in steps 1 through 3.

f. The "PS1" and "PS0" commands have no effect in the ΔV mode. In this mode, the PROBE SWITCH LED is always on or flashing.

3-122. **Signature Collection.** During either of the Signature Analysis modes, the 5005B monitors the gate light. When the gate light goes from on to off, a signature will be collected and is ready for collection by the controller. The controller can read the most current data at any time. If the controller sends the command "GET" or lets the operator press the Data Probe switch, the 5005B will simulate a key press corresponding to the current function settings. A signature will then be collected after the second gate light (two identical consecutive signatures are required for a stable signature).

3-123. COMMAND CODES

3-124. All local functions (with the exception of ALARM VOL) are programmable with individual command codes via the HP-IB. In general, all functions operate in remote the same as in local. The 5005B command codes are described in the following paragraphs. As a quick reference, the program code set is listed (with condensed descriptions), in *Table 3-22.*

3-125. **Function Codes.** The following paragraphs describe the programmable function codes for the 5005B. Bold type denotes the default state on power-up and reset.

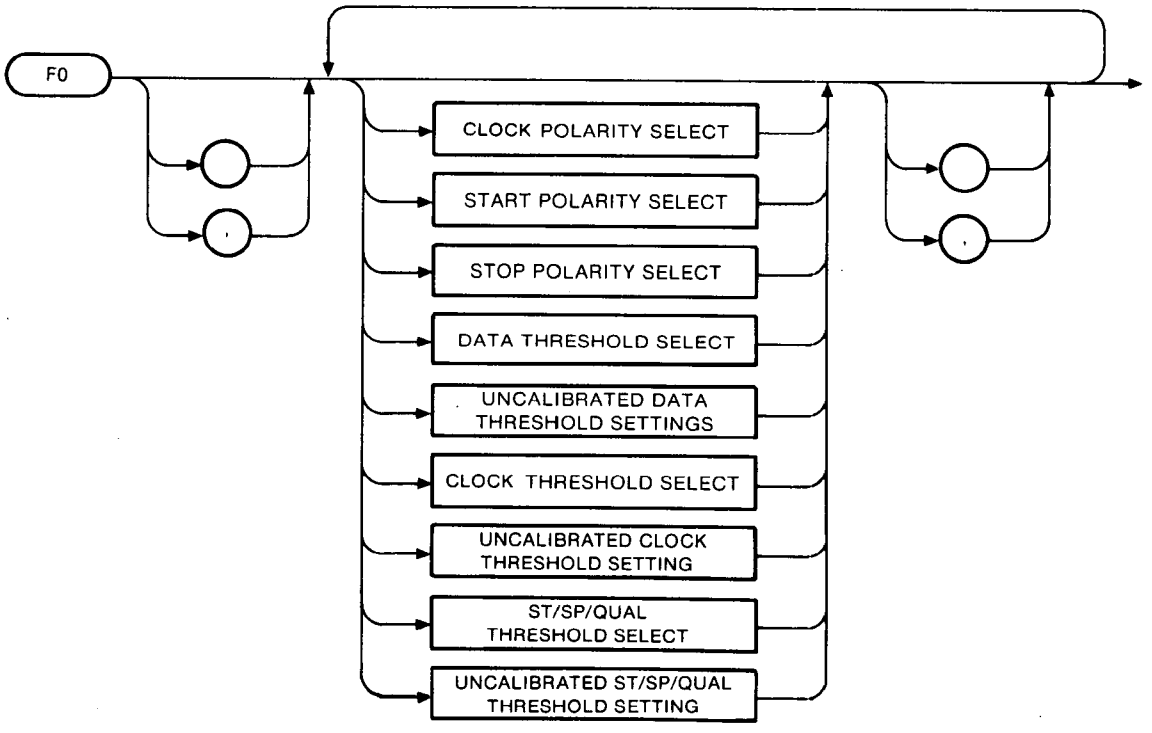
Fn (n=0, 1, 2, . . . 9) Function Select

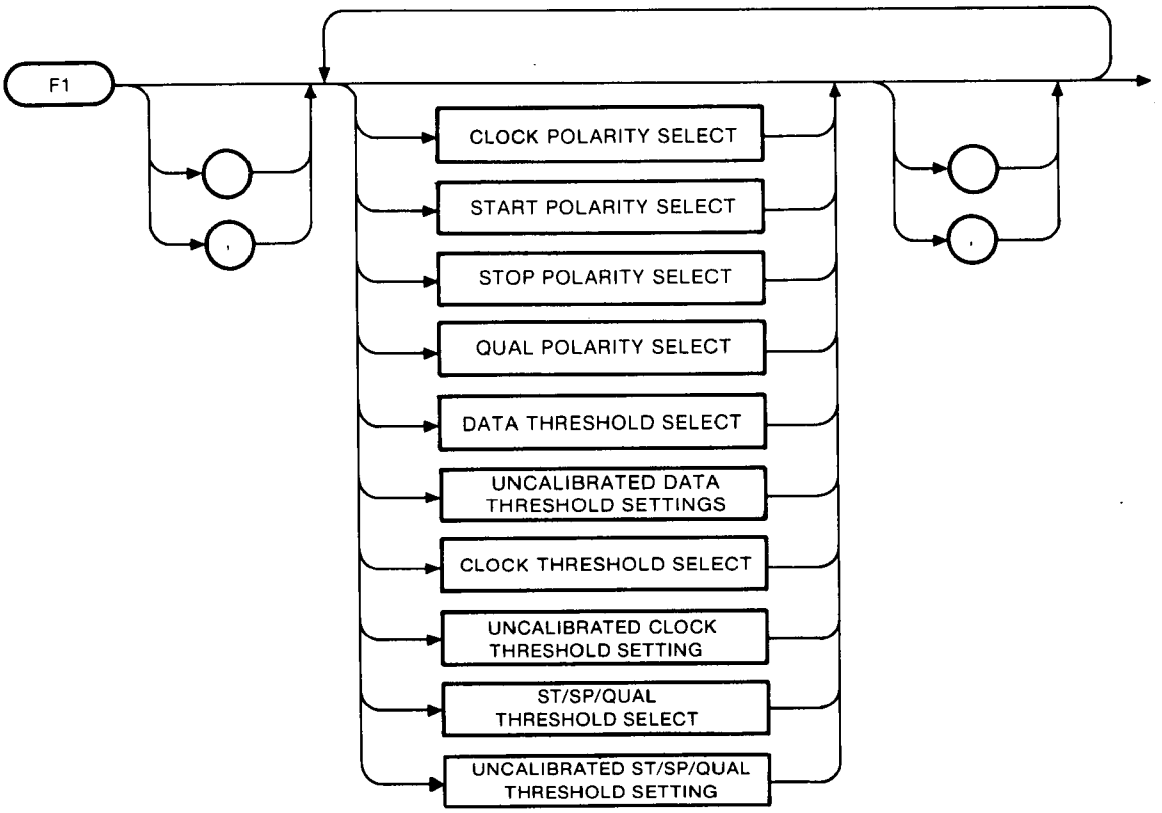
F0 = NORM Signature Analysis
F1 = QUAL Signature Analysis
F2 = Frequency (kHz)
F3 = Totalize (TOTLZ)
F4 = Time Interval (ms)
F5 = Resistance (kΩ)
F6 = DC Voltage (DCV)
*F7 = Difference Voltage (ΔV)
F8 = Positive Peak Voltage (Vp+)
F9 = Negative Peak Voltage (Vp–)

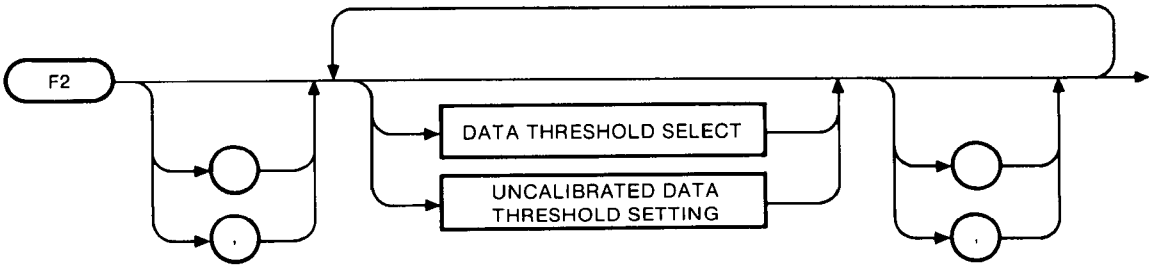
* = Data Probe switch is automatically enabled in this mode.

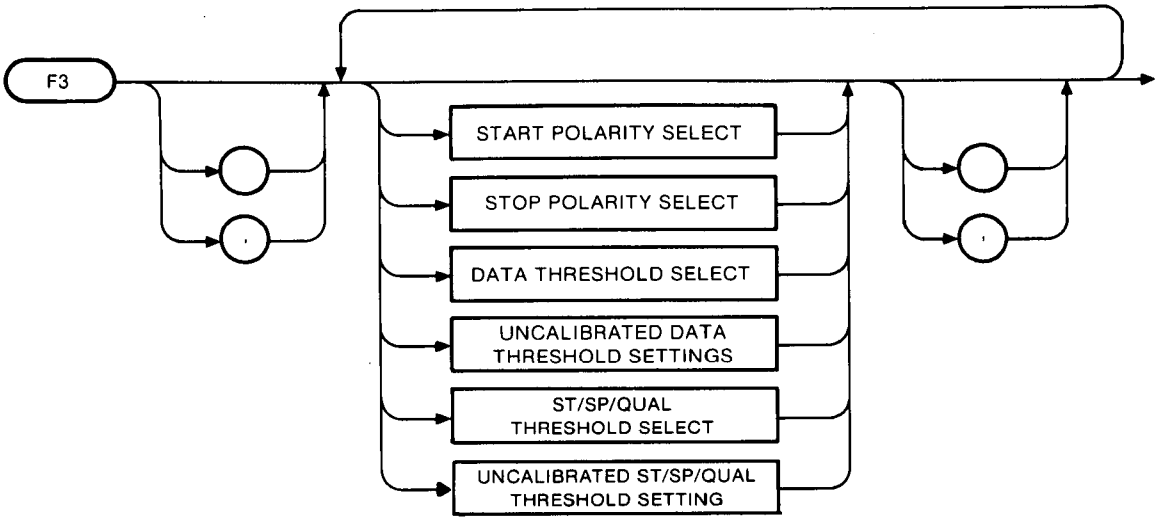
NOTE

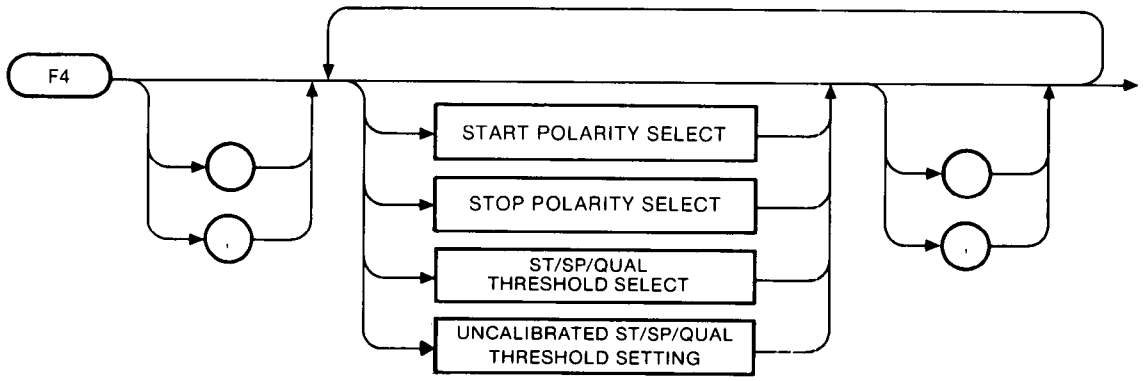
The following syntax diagrams indicate the active front panel parameters which may be programmed for each function. Observe that the names enclosed by a rectangular box refer to commands defined later in this section, and should be replaced by the lower level commands indicated.

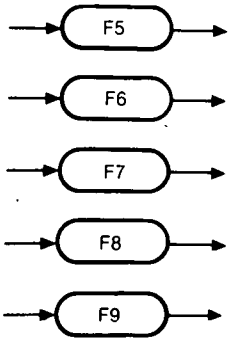



F1
CLOCK POLARITY SELECT
START POLARITY SELECT
STOP POLARITY SELECT
QUAL POLARITY SELECT
DATA THRESHOLD SELECT
UNCALIBRATED DATA THRESHOLD SETTINGS
CLOCK THRESHOLD SELECT
UNCALIBRATED CLOCK THRESHOLD SETTING
ST/SP/QUAL THRESHOLD SELECT
UNCALIBRATED ST/SP/QUAL THRESHOLD SETTING


F2
DATA THRESHOLD SELECT
UNCALIBRATED DATA THRESHOLD SETTING

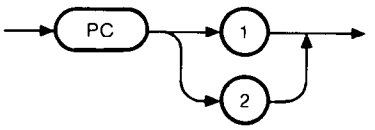

F3
START POLARITY SELECT
STOP POLARITY SELECT
DATA THRESHOLD SELECT
UNCALIBRATED DATA THRESHOLD SETTINGS
ST/SP/QUAL THRESHOLD SELECT
UNCALIBRATED ST/SP/QUAL THRESHOLD SETTING





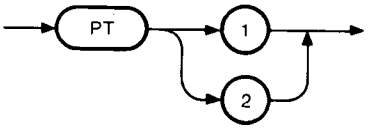
3-126. **Polarity Codes.** The following paragraphs describe the programmable polarity codes for the 5005B. Bold type denotes the default states assumed if the active parameters for a specific function do not occur in the function command string.

PC Clock Polarity Select



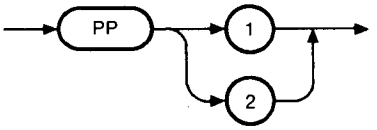
PC1 = Clock triggers on rising edge of signal.
PC2 = Clock triggers on falling edge of signal.

PT Start Polarity Select



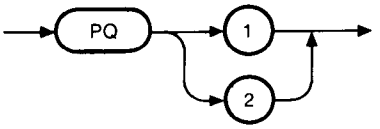
PT1 = Start triggers on rising edge of signal.
PT2 = Start triggers on falling edge of signal.

PP Stop Polarity Select



PP1 = Stop triggers on rising edge of signal.
PP2 = Stop triggers on falling edge of signal.

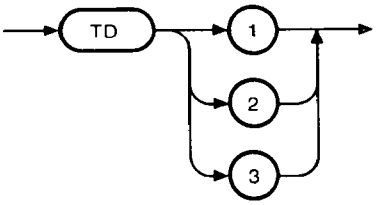
PQ Qualify Polarity Select



PQ1 = Qualify set to active high.
PQ2 = Qualify set to active low.

3-127. **Threshold Codes.** The following paragraphs describe the programmable thresholds codes for the 5005B. Bold type denotes the default states assumed if the active parameters for a specific function do not occur in the function command string.

TD DATA Threshold select

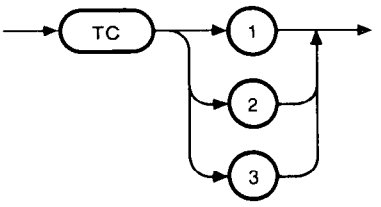


TD1 = DATA thresholds are set to TTL levels.

TD2 = DATA thresholds are set to ECL levels.

TD3 = DATA thresholds are set to 5V CMOS levels.

TC CLOCK Threshold select

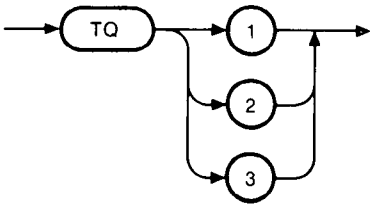


TC1 = CLOCK thresholds are set to TTL levels.

TC2 = CLOCK thresholds are set to ECL levels.

TC3 = CLOCK thresholds are set to 5V CMOS levels.

TQ ST/SP/QUAL Threshold select

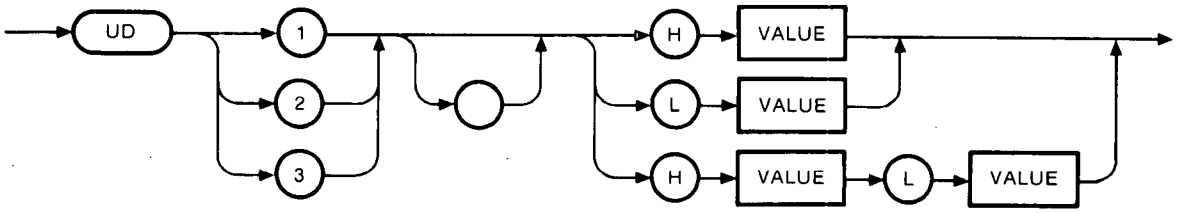


TQ1 = ST/SP/QUAL thresholds are set to TTL levels.

TQ2 = ST/SP/QUAL thresholds are set to ECL levels.

TQ3 = ST/SP/QUAL thresholds are set to 5V CMOS levels.

UD Uncalibrated Data threshold settings



UD1 H±XX.XX L±XX.XX = TTL DATA thresholds are selected to be redefined to uncalibrated levels.

UD2 H±XX.XX L±XX.XX = ECL DATA thresholds are selected to be redefined to uncalibrated levels.

UD3 H±XX.XX L±XX.XX = 5V CMOS DATA thresholds are selected to be redefined to uncalibrated levels.

H = Selects the HIGH threshold to be redefined.

L = Selects the LOW threshold to be redefined.

NOTE

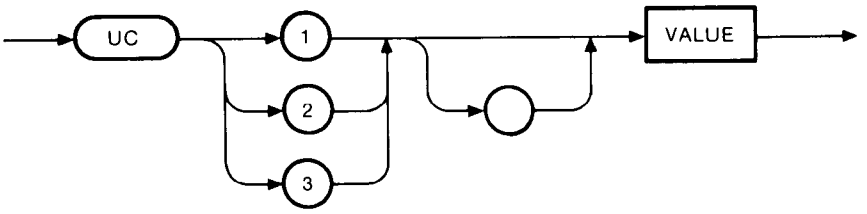
The 5005B will accept H, L, or both settings for this command. Programming standard values into the active threshold will turn off the UNCAL indicator.

VALUE — The range of acceptable threshold values is -12.50 V to +12.50 V. The data must be sent in the following format:

± XX.XX

The "+" sign and the leading "0" are optional. The least significant digit must be either a "0" or a "5". For example, acceptable values are -11.75, 0.05, +03.60, 9.85. Unacceptable values are -13.60 (out of range), 0.6 (no LSB), +03.67 (LSB not 0 or 5), 9 . (no LSB).

UC Uncalibrated CLOCK threshold settings



UC1 ±XX.XX = TTL CLOCK thresholds are selected to be redefined to uncalibrated levels.

UC2 ±XX.XX = ECL CLOCK thresholds are selected to be redefined to uncalibrated levels.

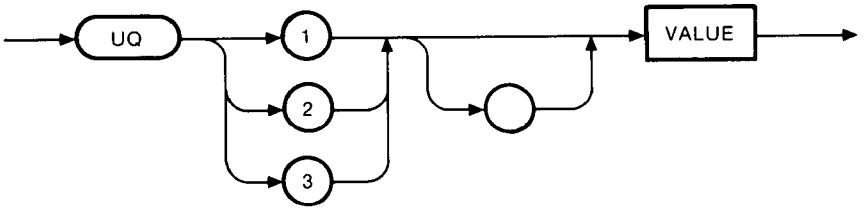
UC3 ±XX.XX = 5V CMOS CLOCK thresholds are selected to be redefined to uncalibrated levels.

VALUE — The range of acceptable threshold values is -12.50 V to +12.50 V. The data must be sent in the following format:

± XX.XX

The "+" sign and the leading "0" are optional. The least significant digit must be either a "0" or a "5". For example, acceptable values are -11.75, 0.05, +03.60, 9.85. Unacceptable values are -13.60 (out of range), 0.6 (no LSB), +03.67 (LSB not 0 or 5), 9 . (no LSB).

UQ Uncalibrated ST/SP/QUAL threshold setting



UQ1 ±XX.XX = TTL ST/SP/QUAL thresholds are selected to be redefined to uncalibrated levels.

UQ2 ±XX.XX = ECL ST/SP/QUAL thresholds are selected to be redefined to uncalibrated levels.

UC3 ±XX.XX = 5V CMOS ST/SP/QUAL thresholds are selected to be redefined to uncalibrated levels.

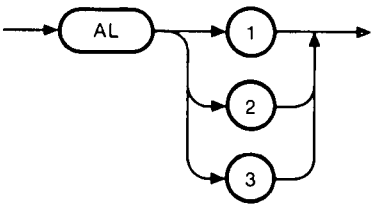
VALUE — The range of acceptable threshold values is -12.50 V to +12.50 V. The data must be sent in the following format:

± XX.XX

The "+" sign and the leading "0" are optional. The least significant digit must be either a "0" or a "5". For example, acceptable values are -11.75, 0.05, +03.60, 9.85. Unacceptable values are -13.60 (out of range), 0.6 (no LSB), +03.67 (LSB not 0 or 5), 9 . (no LSB).

3-128. General Command Codes. The following paragraphs describe the general command codes for the 5005B.

AL Alarm



AL1 = A single audible tone is executed.

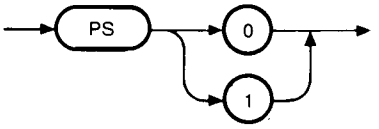
AL2 = A series of three audible tones is executed.

AL3 = A series of ten audible tones is executed.

NOTE

The alarm volume is not alterable via remote HP-IB control. The front panel ALARM VOL key must be pressed to toggle the volume.

PS Probe Switch Enable



PS0 = Probe switch disabled.

PS1 = Probe switch enabled. The PROBE SWITCH LED will be flashing in this state.

3-129. Operation of the Data Probe Switch in Remote

3-130. When the data probe switch is enabled, an operator switch press will execute a measurement in a manner similar to the bus TRIGGER command. When the probe switch is enabled, the yellow PROBE SWITCH status LED will flash. This directs the operator to position the Data Probe tip to a test node indicated by the controller, and press the data probe switch to initiate the measurement. After the data probe switch has been pressed, the PROBE SWITCH status LED will change (from flashing) to on, until the measurement data is read by the controller. Once the data probe switch is pressed, the controller can acquire data from the 5005B as often as it needs.

NOTE

In the ΔV and TALK ONLY modes, the data probe switch is always enabled.

RS Reset 

Causes the 5005B to default to its power-up conditions of:

FUNCTION	SIGNATURE (NORM)
CLOCK POLARITY	Positive edge
START POLARITY	Positive edge
STOP POLARITY	Positive edge
DATA THRESHOLDS	TTL
CLOCK THRESHOLD	TTL
ST/SP/QUAL THRESHOLD	TTL
PROBE SWITCH	disabled
SERVICE REQUEST MASK	cleared

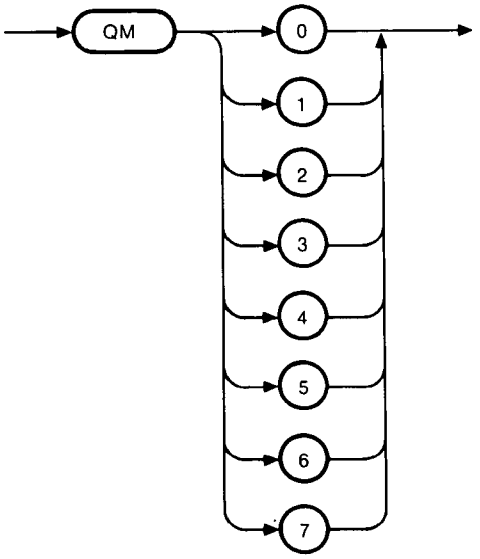
For example, the following command codes are set upon execution of the RS command:

F0, PC1, PT1, PP1, TD1, TC1, TQ1, PS0, QM0

RS can be sent as the leading code in a command string. This initialization clears all settings to default states and only the codes following in the command string can change the operating mode from the default states.

3-131. Service Request Mask. The conditions which cause the 5005B to request service are defined by the setting of the Service Request Mask. The controller sets the Service Request Mask by sending one of the "QM" commands listed below. The digit following the QM command specifies the condition or conditions which will cause the 5005B to request service.

QMn (n=0,1,2,...7) Set Service Request Mask



QM0 = Clear service request mask
QM1 = Data ready for collection
QM2 = Probe switch pushed
QM3 = Data ready **or** probe switch pushed
QM4 = Error condition has occurred
QM5 = Error condition **or** data ready
QM6 = Error condition **or** probe switch pushed
QM7 = Error condition **or** data ready **or** probe switch pushed

3-132. When the 5005B detects the specific conditions defined by the service request mask, the SRQ flag is set, sending an interrupt to the controller. The 5005B Status byte contains information which identifies the service request condition, as shown in *Table 3-20.* A decimal number equivalent to the sum of the different status bits is sent in response to the service request.

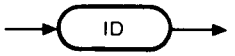
Table 3-20. 5005B Service Request Bits

D7	D6	D5	D4	D3	D2	D1	D0
0					ERROR	PROBE SWITCH PUSHED	DATA READY
128	64	32	16	8	4	2	1

The controller will be interrupted if the SRQ mask is set and one of these situations occurs.

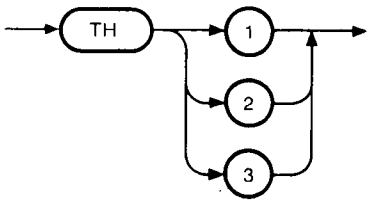
3-133. Output Codes: The following paragraphs describe the programmable output command codes for the 5005B.

ID Identification



Causes the 5005B to respond with HP5005B CR LF. This command is useful for ascertaining the address of the 5005B or for determining which instrument has been assigned to a particular talk/listen address.

TH Threshold value reading



TH1 = Returns the current DATA threshold settings. The format is: H±XX.XX L±XX.XX CR LF.

TH2 = Returns the current CLOCK threshold settings. The format is: ±XX.XX CR LF.

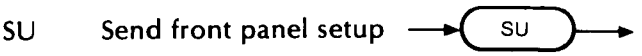
TH3 = Returns the current ST/SP/QUAL threshold settings. The format is ±XX.XX CR LF.

NOTE

If the user is interested in determining the level select (TTL, ECL, 5V CMOS) of the returned threshold, the front panel setup can be read using the "SU" command.

SE Send error code

Causes the 5005B to send the error code to the controller. This code is a decimal representation of the error causing the display to show "Err 15" and the alarm to sound. *Table 3-19* lists the error codes and their meaning.

SU Send front panel setup 

Causes the 5005B to read the current front panel setup and send this information to the controller. The 5005B returns four bytes with binary coded information in addition to CR and LF (bytes 5 and 6). *Table 3-21* explains the format of the returned information and the interpretation of the binary coding.

Table 3-21. Reading Front Panel Setups

The terse command "SU" causes the 5005B to read the current front panel setup and return the information to the controller, encoded in binary, in six consecutive bytes. To illustrate, consider the following example.

The controller (85A) sends the command sequence:

```
10   OUTPUT 703; "SU"          Write to device 03, "Send Front Panel Setup"

20   FOR I=1 TO 6              Read back a byte of binary coded data and assign
30   ENTER 703 USING "#,B";A   to variable "A". Display the value of "A" (in decimal)
40   DISP A                    and loop back until six bytes are displayed.
50   NEXT I
60   END
```

The 5005B will send back six bytes of data, the first four contain the status of the front panel settings encoded in binary as shown below. The last two bytes are a CR and LF.

1st byte (FUNCTION)

128	64	32	16	8	4	2	1
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

0 - 9 = F0 - F9
1 = PS1 command active
2 = PS0 command active
1 = uncalibrated LED on
0 = uncalibrated LED off

2nd byte (POLARITY SELECTION)

128	64	32	16	8	4	2	1
D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1
QUAL		STOP		START		CLOCK	

00 = OFF
01 = ⎍
10 = ⎏

Table 3-21. Reading Front Panel Setups (cont)

3rd byte (THRESHOLD SELECTION)

128 D7	64 D6	32 D5	16 D4	8 D3	4 D2	2 D1	1 D0
		0	1	0	1	0	1
		ST/SP/QUAL		CLOCK		DATA	

00 = OFF
01 = TTL
10 = ECL
11 = CMOS

4th byte (SRQ MASK)

128 D7	64 D6	32 D5	16 D4	8 D3	4 D2	2 D1	1 D0
					0	0	0
					Error	Probe switch pushed	Data Ready

0 = NO
1 = YES

5th byte (CARRIAGE RETURN)

128 D7	64 D6	32 D5	16 D4	8 D3	4 D2	2 D1	1 D0
0	0	0	0	1	1	0	1

6th byte (LINE FEED)

128 D7	64 D6	32 D5	16 D4	8 D3	4 D2	2 D1	1 D0
0	0	0	0	1	0	1	0

NOTE

During the panel setup reading, if the probe switch is enabled, the PROBE SWITCH LED will stop flashing until the reading has been completed.

Table 3-22. HP-IB Program Code Set

Measurement Functions
F0 .....Signature Analysis NORM
F1 .....Signature Analysis QUAL
F2 .....Frequency
F3 .....Totalize
F4 .....Time Interval
F5 .....Resistance
F6 .....DC Voltage
F7 .....Differential Voltage
F8 .....Peak Voltage Positive
F9 .....Peak Voltage Negative

POLARITY SELECT
PC1 .....Set CLOCK to rising slope
PC2 .....Set CLOCK to falling slope
PT1 .....Set START to rising slope
PT2 .....Set START to falling slope
PP1 .....Set STOP to rising slope
PP2 .....Set STOP to falling slope
PQ1 .....Set QUAL to active high
PQ2 .....Set QUAL to active low

THRESHOLD SELECT
Threshold Family Select
TD1 .....Set DATA threshold to TTL
TD2 .....Set DATA threshold to ECL
TD3 .....Set DATA threshold to 5V CMOS
TC1 .....Set CLOCK threshold to TTL
TC2 .....Set CLOCK threshold to ECL
TC3 .....Set CLOCK threshold to 5V CMOS
TQ1 .....Set ST/SP/QUAL threshold to TTL
TQ2 .....Set ST/SP/QUAL threshold to ECL
TQ3 .....Set ST/SP/QUAL threshold to 5V CMOS

Setting Uncalibrated Thresholds
UD1 (values) .....DATA Probe thresholds to TTL values high (H±XX.XX), low (L±XX.XX)
UD2 (values) .....DATA Probe thresholds to ECL values high (H±XX.XX), low (L±XX.XX)
UD3 (values) .....DATA Probe thresholds to 5V CMOS values high (H±XX.XX), low (L±XX.XX)
UC1 (value) .....CLOCK threshold to specified TTL value (±XX.XX)
UC2 (value) .....CLOCK threshold to specified ECL value (±XX.XX)
UC3 (value) .....CLOCK threshold to specified 5V CMOS value (±XX.XX)
UQ1 (value) .....ST/SP/QUAL threshold to specified TTL value (±XX.XX)
UQ2 (value) .....ST/SP/QUAL threshold to specified ECL value (±XX.XX)
UQ3 (value) .....ST/SP/QUAL threshold to specified 5V CMOS value (±XX.XX)

GENERAL CODES
Reset
RS .....Reset: Sets the 5005B to power on conditions; F0, PC1, PP1, PT1, TD1, TC1, TQ1, PS0, and QM0

Data Probe Switch
PS0 .....Data Probe Switch disabled
PS1 .....Data Probe Switch enabled (causing PROBE SWITCH LED to flash)

Alarm
AL1 .....Execute a single audible tone (beep)
AL2 .....Execute three audible tones (beeps)
AL3 .....Execute ten audible tones (beeps)

Table 3-22. HP-IB Program Code Set (cont)

SERVICE REQUEST MASK

QM0 .....Clear service request mask
QM1 .....Data ready for collection
QM2 .....Probe switch pushed
QM3 .....Data ready **or** probe switch pushed
QM4 .....Error condition has occurred
QM5 .....Error condition **or** data ready
QM6 .....Error condition **or** probe switch pushed
QM7 .....Error condition **or** data ready **or** probe switch pushed

OUTPUT CODES

ID .....Identification: Causes identification response "HP5005B" CR LF

TH1 .....Causes 5005B to respond with current DATA threshold settings
TH2 .....Causes 5005B to respond with current CLOCK threshold setting
TH3 .....Causes 5005B to respond with current ST/SP/QUAL threshold setting

SE .....Send Error: Causes the 5005B to respond with a decimal representation of the specific error which produced the Err15 display
SU .....Setups: Causes the 5005B to respond with 4 bytes of binary coded data representing the current setup status of the front panel, plus a CR and LF

NOTE

Power-on default values are shown in bold type.

3-134. PROGRAMMING EXAMPLES

3-135. The following examples demonstrate programming capabilities of the 5005B. The examples are written for the HP85A controller, and illustrate function selection, service request, reading the front panel setup, reading the status byte, and instrument identification. A summary of the example program operation and a line-by-line description are provided.

3-136. The first three examples listed in this section assume a 5005B address setting of "03" (address switches to "0000011"). The 5005B is addressed to talk and listen by using the code "703" where "03" is the 5005B address and "7" is the interface select code. The ASCII characters for the same switch settings are "C" for a talk address and "#" for a listen address. These characters would be used if the controller were an HP9830A calculator (or 9825A/B when using the "cmd" statement).

3-137. Special Programming Considerations

3-138. To clarify programming of the 5005B, the following considerations should be noted:

a. If the 5005B is in remote and the controller sends the "local" command, all subsequent local settings will remain intact when the controller places the 5005B in remote again. If the 5005B is in remote and the operator presses the "LOCAL" key, all the remote settings (except for threshold voltages) will be recalled when the controller places the 5005B in remote again.

b. During HP-IB operation with the Data Probe switch enabled, pressing the "LOCAL" key will bring the 5005B temporarily to the local mode. This allows the 5005B to make manual measurements. At the end of manual operation, the operator can press the Data Probe switch to recover the settings prior to the manual mode and resume automatic testing. In this manner, the operator can interrupt the automatic test procedure without interrupting the test sequence.

c. When a hardware or software error occurs, the 5005B goes into an error mode. The "LOCAL" key will bring the 5005B back to normal operation.

d. If a command is sent to the 5005B under remote control, and the 5005B is busy, the command will remain on the bus until the 5005B is finished and is free to execute the new command.

EXAMPLE 1 FUNCTION SELECT, PROBE SWITCH PRESS AND MEASUREMENT RETURN

The following example demonstrates the ease with which the 5005B is programmed. A specific function (kΩ) is selected and the probe switch is activated. The program then waits until the operator presses the probe switch, which initiates the measurement. A service request (SRQ) is generated by the switch press which prompts the controller's interrupt service routine to read, then display the resulting measurement value.

```
10 CLEAR
20 REMOTE 703
30 OUTPUT 703 ;"F5 QM2 PS1"
40 DISP "Waiting for probe swit
   ch press."
50 STATUS 7,1 ; Q
60 ON INTR 7 GOTO 90
70 ENABLE INTR 7;8
80 GOTO 80
90 DISP "Measurement taken." @
   BEEP
```

Line 10: Clear HP85 screen.

Line 20: Place 5005B in remote mode.

Line 30: Program function to kΩ, set the service request mask to detect a probe switch press, and enable the probe switch.

Line 40: Display operator prompt message.

Line 50: Clear HP85 Interface Status Register to enable a new interrupt.

Line 60: When an interrupt from the HP-IB Interface is received, program execution will branch to the interrupt service routine (line 90).

Line 70: Enable an interrupt of the HP85 by the HP-IB Interface (7) if SRQ (bit 3, decimal value 8) is sensed.

Line 80: Program loops (remains) at line 80 until interrupt occurs.

Line 90: Display measurement confirmation message and beep.

```
100 ENTER 703 ; A$
110 DISP "The value read is ";A$
    ;" ."
120 DISP "END OF PROGRAM"
130 END
```

Line 100: Read the data value from 5005B.

Line 110: Display the data reading.

Line 120: Display the "END OF PROGRAM" message.

Line 130: End program execution.

To repeat this program, simply press the RUN key. Three possible measurement values are:

a. No connection (open circuit). The display will read "OPEN" and the value returned will be "9.9999 E +19".

b. Probe tip to red, yellow, or green Timing Pod inputs. Display will read approximately 100 (kΩ) and value returned will be approximately "100 E +03".

c. Probe tip to black (ground) Timing Pod input. Display will read "0.000" and value returned will be "0.000 E +03"

EXAMPLE 2 READING FRONT PANEL SETUP

The following example resets the 5005B, then programs a selection of function, polarity, and threshold settings which alter the standard front panel settings. The program sets the 5005B function to SA QUAL, all four polarities to falling edge, DATA thresholds to uncalibrated TTL values, CLOCK threshold to (standard) ECL, and ST/SP/QUAL threshold to (standard) 5V CMOS. After waiting a few seconds, the program sends a "read front panel setup" command. The 5005B returns six bytes of binary data, which are read and displayed by the HP85.

```
10 REMOTE 703
20 OUTPUT 703 ;"RS"
30 OUTPUT 703 ;"F1 PC2 PT2 PP2
   PQ2 UD1 H+2.40 L+0.40 TC2 TQ
   3"
40 OUTPUT 703 ;"SU"
```

Line 10: Place 5005B in remote mode.

Line 20: Reset the 5005B.

Line 30: Program the 5005B to the following conditions:

Function	SA QUAL
CLOCK Polarity	falling edge
START Polarity	falling edge
STOP Polarity	falling edge
QUAL Polarity	active low
DATA Threshold	Uncalibrated TTL levels, H=+2.40 L=+0.40
CLOCK Threshold	ECL (standard) level
ST/SP/QUAL Threshold	5V CMOS (standard) level

Line 40: Instruct the 5005B to send front panel setup information.

```
 50 CLEAR
 60 FOR I=1 TO 6
 70 ENTER 703 USING "#,B" ; A
 80 BEEP @ DISP A @ WAIT 1000
 90 NEXT I
100 END
```

Line 50: Clear HP85 screen.

Line 60: Iterate the following 2 lines 6 times.

Line 70: Read back a byte of binary coded information and assign to variable "A".

Line 80: Beep, display the value of "A", and wait 1 second.

Line 90: Continue step iteration.

Line 100: End program execution.

These are the decimal values which correspond to the front panel setup programmed in line 40. The decimal values were determined from the binary coded bytes, returned by the 5005B, as shown below.

1st byte (FUNCTION)

128 D7	64 D6	32 D5	16 D4	8 D3	4 D2	2 D1	1 D0	
0	1	0	1	0	1	0	1	=33
FUNCTION								

2nd byte (POLARITY SELECTION)

128 D7	64 D6	32 D5	16 D4	8 D3	4 D2	2 D1	1 D0	
0	1	0	1	0	1	0	1	=170
QUAL		STOP		START		CLOCK		

3rd byte (THRESHOLD SELECTION)

128 D7	64 D6	32 D5	16 D4	8 D3	4 D2	2 D1	1 D0	
0	1	0	1	0	1	0	1	=57
		ST/SP/QUAL		CLOCK		DATA		

4th byte (SRQ MASK)

128 D7	64 D6	32 D5	16 D4	8 D3	4 D2	2 D1	1 D0	
0	1	0	1	0	1	0	1	=0

5th byte (CARRIAGE RETURN)

128 D7	64 D6	32 D5	16 D4	8 D3	4 D2	2 D1	1 D0	
0	1	0	1	0	1	0	1	=13

6th byte (LINE FEED)

128 D7	64 D6	32 D5	16 D4	8 D3	4 D2	2 D1	1 D0	
0	1	0	1	0	1	0	1	=10

EXAMPLE 3 READING STATUS BYTE

The following example demonstrates a use of the status byte. The status byte identifies the present state of several conditions within the 5005B. The program example sets the 5005B service request mask to generate an SRQ when one of these conditions changes. The condition monitored is the status of the probe switch, which is enabled and programmed to generate an SRQ when the probe switch is pressed. The program reads the status byte prior to and following the SRQ, to illustrate the response.

```
 10 CLEAR
 20 REMOTE 703
 30 OUTPUT 703 ;"QM2 PS1"
 40 A=SPOLL(703)
 50 DISP "The value of the statu
    s byte    prior to the probe
     switch press is";A;"."
 60 DISP
 70 DISP "Press the probe switch
     to       generate an SRQ an
    d alter the "
 80 DISP "status byte value. "
 90 DISP "Press CONT when ready.
    "
100 PAUSE
110 BEEP
120 A=SPOLL(703)
130 IF A=32 THEN DISP "PROBE SWI
    TCH NOT PUSHED!!!" @ WAIT 25
    00 @ CLEAR @ GOTO 50
140 DISP
150 DISP "The value of the statu
    s byte    after the probe sw
    itch press    is";A;"."
160 DISP
170 DISP "END OF PROGRAM"
180 END
```

Line 10: Clear HP85 screen.

Line 20: Place 5005B in remote mode.

Line 30: Program the 5005B service request mask to detect a probe switch press, and enable the probe switch.

Line 40: Read the status of the 5005B by a serial poll at address 703.

Line 50: Display the value of the status byte.

Line 60: Display a blank line.

Lines 70-90: Message to prompt the user to press the probe switch, then the CONT key when ready.

Line 100: Halt program execution until CONT is pressed.

Line 110: Beep

Line 120: Read the status of the 5005B by a serial poll at address 703.

Line 130: Display error message if probe switch was not pressed, then branch to line 50.

Line 140: Display a blank line.

Line 150: Display the value of the status byte.

Line 160: Display a blank line.

Line 170: Display "END OF PROGRAM" message.

Line 180: End program execution.

When in remote operation, the 5005B can send a service request (SRQ) to controller under any or all of the following condition(s), as defined by the Service Request Mask (QMn command, see paragraph 3-131) must be set prior to the condition.

1. Data ready. A measurement has been completed and data is available for collection.

2. Probe Switch pressed. The probe switch has been pressed to initiate a measurement.

3. Error. An error condition exists.

In general, the controller can read the 5005B status byte at any time to check selected operating conditions, as shown below. For this program example the service request mask has been set to detect a probe switch press. The first reading of the status byte should return a "40", indicating that the power up was successful and the 5005B is performing a command routine. All other conditions would be "0"s. After the probe switch press, the status byte should change to "99", reflecting an SRQ Flag, Power On OK, Probe Switch Pushed, and Data Ready.

D7	D6	D5	D4	D3	D2	D1	D0
0	SRQ FLAG	POWER ON OK	LOCAL	BUSY	ERROR	PROBE SWITCH PUSHED	DATA READY
128	64	32	16	8	4	2	1

A decimal number equivalent to the sum of the different status bits will be sent in response to the status request.

EXAMPLE 4 INSTRUMENT IDENTIFICATION

The following example demonstrates the Instrument Identification (ID) command. The program uses a loop routine to increment through all possible addresses, requesting an instrument identification. When the program reaches the address set on the 5005B, the identification response "HP5005B" is received. The program then displays the "HP5005B FOUND ..." message, and indicates the corresponding address.

```
10 CLEAR
20 DISP "Searching for 5005B ad
   dress..."
30 N$="NOT5B"
40 FOR A=700 TO 730
50 IF A=721 THEN 140
60 DISP A @ BEEP 250,10
70 REMOTE A
```

Line 10: Clear HP85 screen.

Line 20: Display message indicating controller is busy.

Line 30: Initialize identification string.

Line 40: Repeat the following 9 lines 30 times (to access address 00 through 30).

Line 50: Branch to next address if 721 (preset controller address) is encountered.

Line 60: Display present address and beep.

Line 70: Place device at address "A" in remote.

```
 80 SET TIMEOUT 7;250
 90 OUTPUT A ;"ID"
100 ENTER A ; N$
110 IF N$="HP5005B" THEN 210
120 CLEAR A
130 ABORTIO 7
140 NEXT A
150 BEEP @ BEEP
160 CLEAR @ DISP "Address not fo
    und."
170 DISP @ DISP "Verify HP-IB co
    nnection and thatthe 5005B i
    s not in the TALK    ONLY mo
    de."
180 DISP @ DISP "Press CONT when
     ready."
190 PAUSE
200 GOTO 10
210 BEEP @ DISP "HP5005B FOUND A
    T ADDRESS";A;"!"
220 END
```

Line 80: Set timeout of interface (7) to 250ms (handshaking must occur within this time period).

Line 90: Send "ID" command to presently addressed device.

Line 100: Read from the device at address "A", the returned response (if any).

Line 110: Branch to line 210 if the response string is "HP5005B" (indicating the HP5005B has been found).

Line 120: Clear the device at listen address "A" (if any errors have been generated).

Line 130: Abort I/O operations for interface select code 7.

Line 140: Continue step iteration.

Line 150: Beep two times.

Lines 160-180: Clear HP85 screen and display message indicating that the address of the HP5005B has not been found. Suggest possible causes and prompt user to press CONT when ready to proceed.

Line 190: Halt program execution until CONT key is pressed.

Line 200: Branch to line 10 and repeat search.

Line 210: Beep and display message indicating at which address the HP5005B has been found.

Line 220: End program execution.

QUICK REFERENCE SHEET

HP-IB Program Code Set

MEASUREMENT FUNCTIONS

F0 .....Signature Analysis NORM
F1 .....Signature Analysis QUAL
F2 .....Frequency
F3 .....Totalize
F4 .....Time Interval
F5 .....Resistance
F6 .....DC Voltage
F7 .....Differential Voltage
F8 .....Peak Voltage Positive
F9 .....Peak Voltage Negative

THRESHOLD SELECT

Threshold Family Select

TD1 .....Set DATA threshold to TTL
TD2 .....Set DATA threshold to ECL
TD3 .....Set DATA threshold to 5V CMOS
TC1 .....Set CLOCK threshold to TTL
TC2 .....Set CLOCK threshold to ECL
TC3 .....Set CLOCK threshold to 5V CMOS
TQ1 .....Set ST/SP/QUAL threshold to TTL
TQ2 .....Set ST/SP/QUAL threshold to ECL
TQ3 .....Set ST/SP/QUAL threshold to 5V CMOS

POLARITY SELECT

PC1 .....Set CLOCK to rising slope
PC2 .....Set CLOCK to falling slope
PT1 .....Set START to rising slope
PT2 .....Set START to falling slope
PP1 .....Set STOP to rising slope
PP2 .....Set STOP to falling slope
PQ1 .....Set QUAL to active high
PQ2 .....Set QUAL to active low

GENERAL CODES

Reset

RS .....Reset: Sets the 5005B to power on conditions; F0, PC1, PP1, PT1, TD1, TC1, TQ1, PS0, and QM0

Data Probe Switch

PS0 .....Data Probe Switch disabled
PS1 .....Data Probe Switch enabled (causing PROBE SWITCH LED to flash)

Alarm

AL1 .....Execute a single audible tone (beep)
AL2 .....Execute three audible tones (beeps)
AL3 .....Execute ten audible tones (beeps)

Setting Uncalibrated Thresholds

UD1 (values) .....DATA thresholds to TTL values high (H±XX.XX), low (L±XX.XX)
UD2 (values) .....DATA thresholds to ECL values high (H±XX.XX), low (L±XX.XX)
UD3 (values) .....DATA thresholds to 5V CMOS values high (H±XX.XX), low (L±XX.XX)
UC1 (value) .....CLOCK threshold to specified TTL value (±XX.XX)
UC2 (value) .....CLOCK threshold to specified ECL value (±XX.XX)
UC3 (value) .....CLOCK threshold to specified 5V CMOS value (±XX.XX)
UQ1 (value) .....ST/SP/QUAL threshold to specified TTL value (±XX.XX)
UQ2 (value) .....ST/SP/QUAL threshold to specified ECL value (±XX.XX)
UQ3 (value) .....ST/SP/QUAL threshold to specified 5V CMOS value (±XX.XX)

SERVICE REQUEST MASK

QM0 .....Clear service request mask
QM1 .....Data ready for collection
QM2 .....Probe switch pushed
QM3 .....Data ready **or** probe switch pushed
QM4 .....Error condition has occurred
QM5 .....Error condition **or** data ready
QM6 .....Error condition **or** probe switch pushed
QM7 .....Error condition **or** data ready **or** probe switch pushed

OUTPUT CODES

ID .....Identification: Causes identification response "HP5005B" CR LF

TH1 .....Causes 5005B to respond with current DATA threshold settings
TH2 .....Causes 5005B to respond with current CLOCK threshold setting
TH3 .....Causes 5005B to respond with current ST/SP/QUAL threshold setting

SE .....Send Error: Causes the 5005B to respond with a decimal representation of the specific error which produced the Err15 display
SU .....Setups: Causes the 5005B to respond with 4 bytes of binary coded data representing the current setup status of the front panel, plus a CR and LF

Quick Reference Sheet (Continued)

5005B Status Byte

D7	D6	D5	D4	D3	D2	D1	D0
0	SRQ FLAG	POWER ON OK	LOCAL	BUSY	ERROR	PROBE SWITCH PUSHED	DATA READY
128	64	32	16	8	4	2	1

Output Data Format

Signature	XXXX		CR	LF	
Frequency	XX.X.X.X.	E+3	CR	LF	
Totalize	XXXXX	E+0	CR	LF	
Time Interval	X.X.X.X.X.	E-3	CR	LF	
kΩ	XX.X.X.X	E+3	CR	LF	Open circuit: 9.9999 E19 CR LF
DCV	(-)XX.X.XX	E+0	CR	LF	
ΔV	(-)XX.X.XX	E+0	CR	LF	
VP+	(-) XX.XX	E+0	CR	LF	
Vp-	(-) XX.XX	E+0	CR	LF	
Overflow	9.9999	E+09	CR	LF	
Error	9	E29	CR	LF	

5005B Error Message Codes

HP-IB Command and Operation Related Errors	
Error 81	Command string too long (over 250 characters).
Error 82	No match for HP-IB command. Implies illegal or incomplete HP-IB command.
Error 83	Illegal or missing numeric trailer in HP-IB command.
Error 84	Attempted selection of an edge select or threshold select not active in this function.
Error 85	HP-IB IC (8291) "Err" bit set. Implies no active listeners on the bus. Controller error.
Error 86	Illegal threshold voltage command format.
Error 87	Programmed threshold voltage out of range.
Error 88	Local key pushed and some function other than delta volts selected after remote selection of delta volts. The delta volts reference is no longer valid, resulting in the possibility of erroneous data being sent to the controller.

SECTION IV
PERFORMANCE TESTS

4-1. INTRODUCTION

4-2. The procedures in this section provide a quick method of verifying the basic operation of the 5005B Signature Multimeter. The tests can be performed to give a high degree of confidence that the 5005B is performing properly. All tests can be performed without access to the interior of the instrument. The Operation Verification tests the standard functions of the instrument in both local and remote modes.

4-3. EQUIPMENT REQUIRED

4-4. The equipment required for the operation verification procedure is listed in *Table 1-2*. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model numbers.

4-5. CALIBRATION CYCLE

4-6. The 5005B requires periodic verification of operation. Depending on the use and environmental conditions, the 5005B should be checked using the operation verification procedure at least once every year.

4-7. TEST RECORD

4-8. Results of the Operation Verification Tests may be tabulated on *Table 4-2*, Operation Verification Test Record, located at the end of the procedures.

4-9. OPERATION VERIFICATION PROCEDURES

4-10. Self-Check

a. Before switching on the instrument, ensure that the power cord is properly attached, the correct fuse is installed, and all safety precautions have been observed.

b. Set LINE OFF-ON switch to ON and verify the Self-Check routine as follows: Upon applying power, all front panel LEDs, except GATE and UNSTABLE, should light momentarily. GATE and UNSTABLE should randomly flash on and off, and the 5005B display should be "-8.8.8.8.8.". After approximately three seconds, verify that an audible tone (beep) is heard, four lighted bars (the center segments of the four rightmost display LEDs) are displayed, and the NORM key indicator, CLOCK, START, STOP rising edge, and all TTL level LED indicators are lighted. Verify that all other LEDs are unlighted.

c. Record results on operation verification test record, *Table 4-2*.

4-11. Polarity Edge Select Verification

a. Proper operation will be checked by toggling the CLOCK, START, STOP, and QUAL trigger edges, and verifying the front panel status LEDs.

b. Press the 5005B front panel QUAL Signature Analysis pushbutton.

c. Press the 5005B front panel CLOCK polarity pushbutton and verify that the trigger edge status LED toggles. Press the same polarity pushbutton and verify that the trigger edge status LED returns to the original position.

d. Repeat step c for the START, STOP, and QUAL polarity pushbuttons.

e. Record results on operation verification test record, *Table 4-2.*

4-12. Threshold Family Select

a. Proper operation will be checked by scrolling through the three logic families for the DATA, CLOCK, and ST/SP/QUAL thresholds, and verifying the front panel status LEDs.

b. Press the 5005B front panel QUAL Signature Analysis pushbutton.

c. Press the 5005B front panel DATA threshold pushbutton:

once — to view the high threshold value
again — to view the low threshold value
once more — to change the logic family and view the high threshold value.

Continue pressing the DATA threshold pushbutton and verify that the lighted LED returns to its original position.

d. Press the 5005B front panel CLOCK threshold pushbutton:

once — to view the threshold value
again — to change the logic family and view the threshold value.

Continue pressing the CLOCK threshold pushbutton and verify that the lighted LED returns to its original position.

e. Repeat step d for the ST/SP/QUAL threshold pushbutton.

f. Record results on operation verification test record, *Table 4-2.*

4-13. Noise MRG Adjust Verification

a. Proper operation will be checked by slewing a TTL CLOCK threshold value up, then down and observing the display.

b. Press the 5005B front panel QUAL Signature Analysis pushbutton.

c. Press the 5005B front panel CLOCK threshold pushbutton to momentarily display the threshold value.

d. **While the threshold value is displayed,** press and hold the 5005B front panel Noise MRG Adjust "up arrow" pushbutton for ≈2 seconds and verify that the displayed threshold value slews up (positive) in 0.05V steps.

e. **While the threshold value is displayed,** press and hold the 5005B front panel Noise MRG Adjust "down arrow" pushbutton for ≈2 seconds. Verify that the displayed threshold value slews down (negative) in 0.05V steps.

f. Record results on operation verification test record, *Table 4-2.*

4-14. Data Probe Switch Verification

a. Proper operation will be checked by pressing the Data Probe switch in the ΔV mode and verifying the front panel status LED.

b. Press the 5005B front panel ΔV pushbutton and verify that the front panel PROBE SWITCH status LED begins flashing.

c. Press the switch on the Data Probe and verify that the front panel PROBE SWITCH status LED remains lighted for approximately two seconds, then resumes flashing.

d. Record results on operation verification test record, *Table 4-2.*

4-15. Frequency Counter Verification

a. Proper operation will be checked by applying a signal of a specific frequency and amplitude and verifying that the 5005B displays the correct frequency.

b. Connect equipment as shown in *Figure 4-1.*

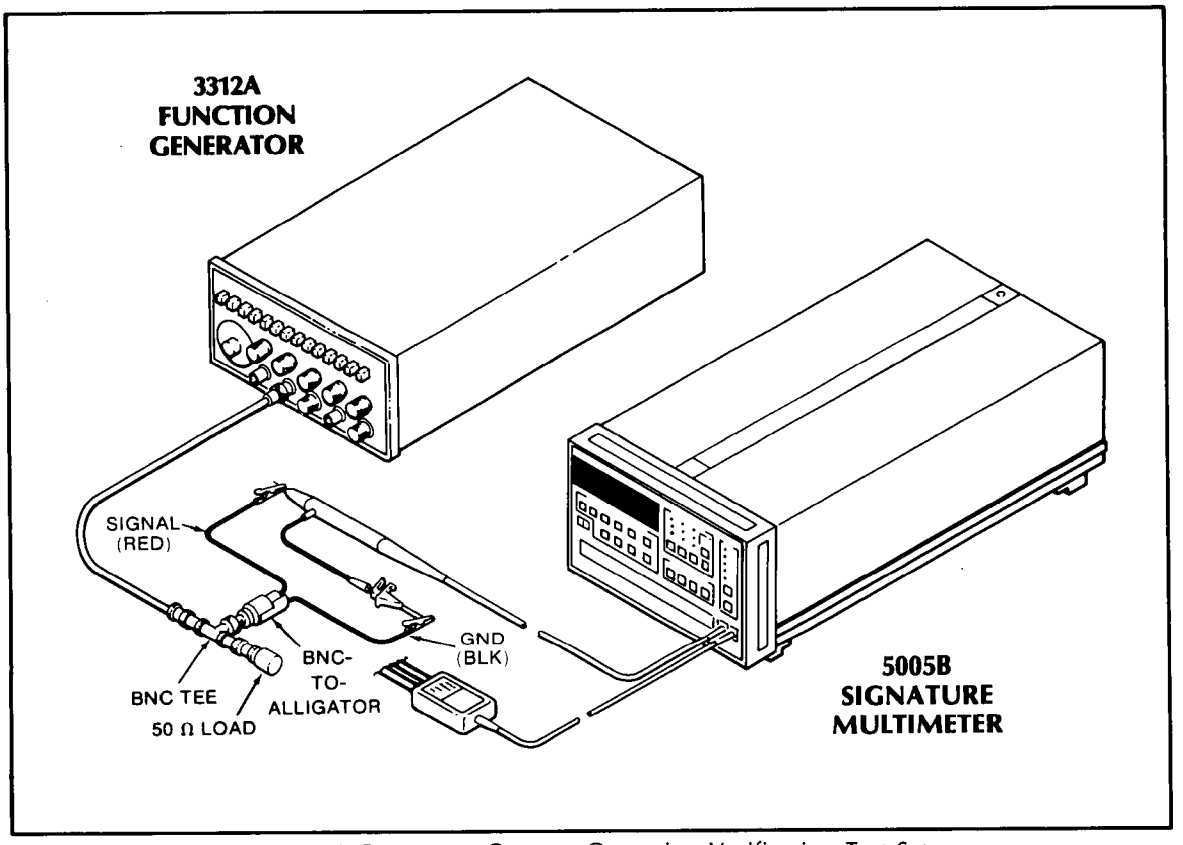


Figure 4-1. Frequency Counter Operation Verification Test Setup

c. With the 3312A LINE switch to "OFF", press the 5005B front panel **kHz** pushbutton. The display should read " 0.000 ", the GATE LED should flash every second, and the DATA THRESHOLD TTL LED should be lighted. All other LEDs should be unlighted.

d. Set the 3312A LINE switch to "ON", and adjust the output for a 10 Hz square wave with an amplitude of 10V (-5V to +5V).

e. Connect the Data Probe to the 3312A and verify that the 5005B displays ~" 00 10 " with all LED indications the same as in step c. The Data Probe light should be flashing.

f. Set the 3312A to output a 2 MHz square wave with an amplitude of 10V (-5V to +5V).

g. Connect the Data Probe to the 3312A and verify that the 5005B displays ~"2000.0" with all LED indications the same as in step c. The Data Probe light should be flashing.

h. Record results on operation verification test record, *Table 4-2.*

4-16. Totalizing Counter Verification

a. Proper operation will be checked by applying a signal of a specific frequency and amplitude and verifying that the 5005B displays a correct totalized indication.

b. Connect equipment as shown in *Figure 4-2.*

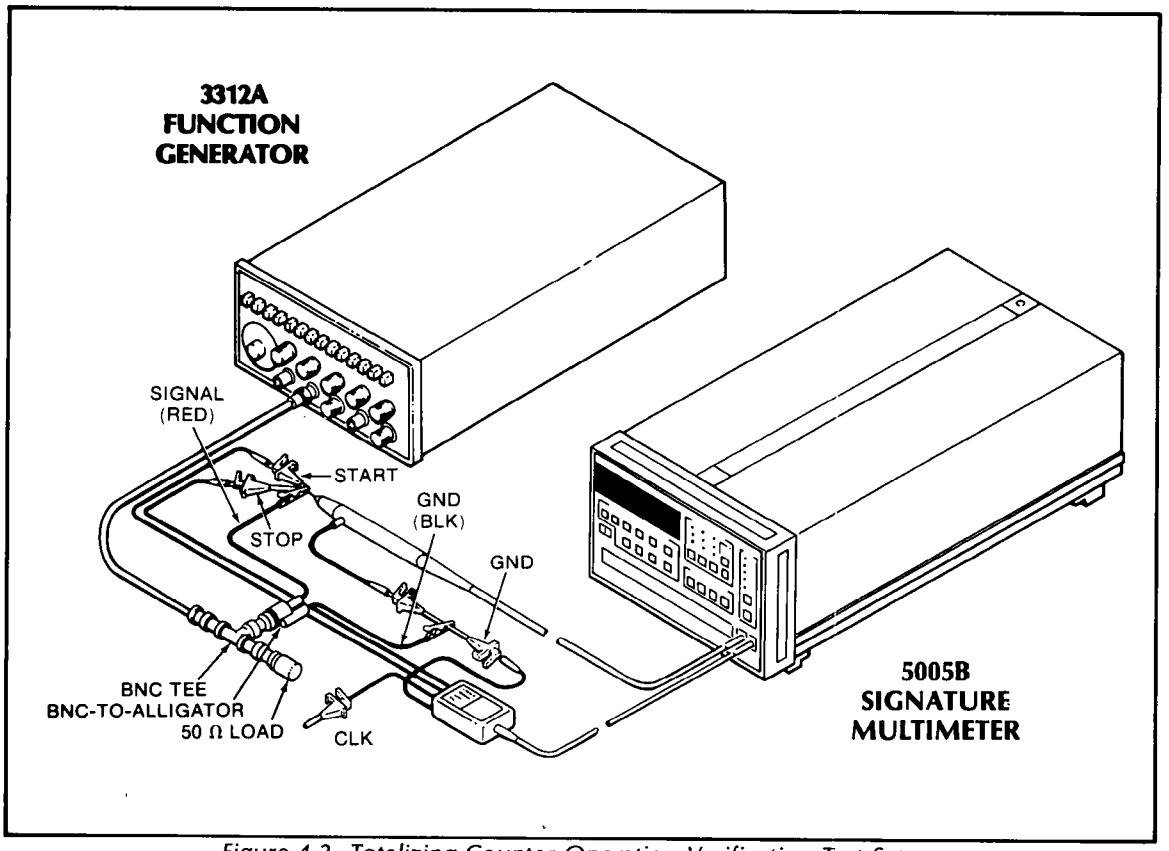


Figure 4-2. Totalizing Counter Operation Verification Test Setup

c. Press the 5005B front panel **TOTLZ** pushbutton. Verify that (with no input applied) four lighted bars are displayed, the THRESHOLD DATA and ST/SP/QUAL TTL LEDs, and the POLARITY START and STOP rising edge LEDs are lighted. All other LEDs should be unlighted.

d. Set the 3312A to output a 100 Hz square wave with an amplitude of 10V (-5V to +5V).

e. Set the START and STOP POLARITY edge selects to the ⅂ position.

f. Connect the Data Probe and the START/ST/SP (green) and STOP/QUAL (red) Pod test leads to the 3312A. Verify that the display reads "0001" with the GATE LED flashing, and all other LED indications the same as in step c.

NOTE

A more visual demonstration of TOTLZ can be performed by momentarily touching the START/ST/SP (green) lead to the 3312A output, waiting a few seconds, then touching the STOP/QUAL (red) lead. The display will register the number of events, representative of the input frequency and amount of time between the Start and Stop signals.

g. Record results on operation verification test record, *Table 4-2.*

4-17. Time Interval Verification

a. Proper operation will be checked by applying a signal of a specific frequency and amplitude and verifying that the 5005B displays the correct time interval indication.

b. Connect equipment as shown in *Figure 4-3*.

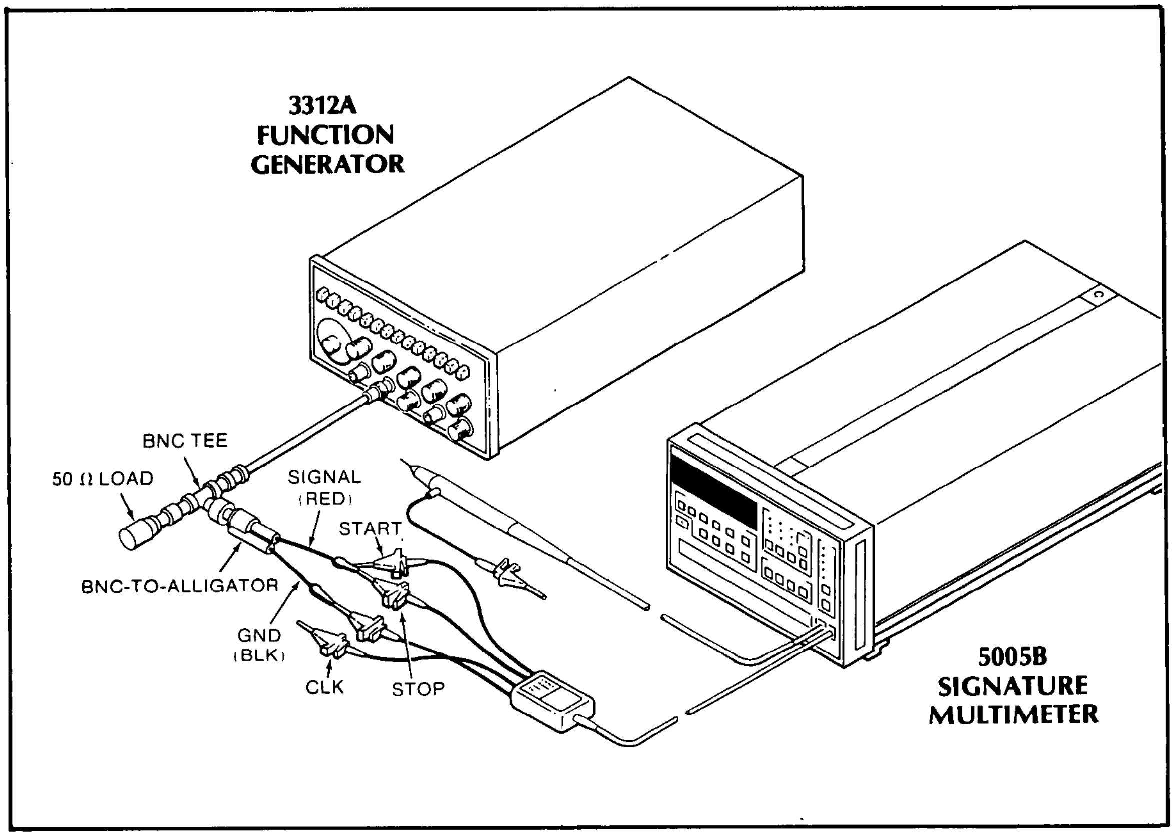


Figure 4-3. Time Interval Operation Verification Test Setup

c. Press the 5005B front panel **ms** pushbutton. Verify that (with no input applied) four lighted bars are displayed, the SP/ST/QUAL, THRESHOLD TTL, and POLARITY START and STOP rising edge LEDs are lighted. All other LEDs should be unlighted.

d. Set the 3312A to output a 100 Hz square wave with an amplitude of 10V (−5V to +5V).

e. Verify that the START and STOP POLARITY edge selects are set to the ⨍ position.

f. With the START/ST/SP (green) and STOP/QUAL (red) Pod test leads connected to the 3312A, verify that the display reads ≈"10.000." with the GATE LED flashing, and all other LED indications the same as in step c.

g. Record results on operation verification test record, *Table 4-2*.

4-18. Ohmmeter Verification

a. Proper operation will be checked by connections from the Data Probe to the Pod, verifying the ground continuity and input impedance to the Pod and to the Data Probe.

b. Press the 5005B front panel **kΩ** pushbutton. Before connecting the Data Probe to any lead, verify that the kΩ LED is lighted and the display reads " OPEN ".

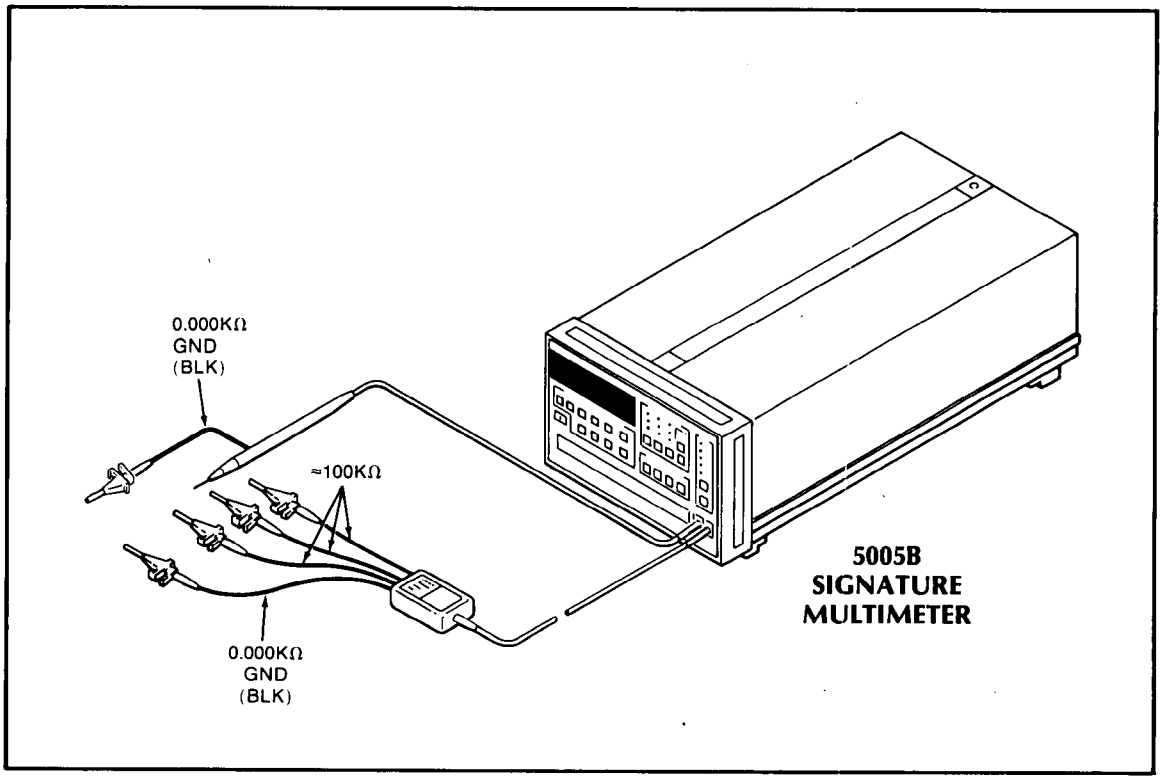


Figure 4-4. Ohmmeter Operation Verification Test Setup

c. Connect the Data Probe tip to the Data Probe ground (⊥) lead. Verify that the display reads " 0.000 " ±0.002.

d. Connect the Data Probe tip to the Pod ground (⊥) lead. Verify that the display reads " 0.000 " ±0.002.

e. Connect the Data Probe tip to the Pod START/ST/SP, STOP/QUAL, and CLOCK test leads sequentially. Verify that the display reads ~" 100.0 " kΩ for each connection.

f. Connect the Data Probe tip to the Data Probe ground (⊥) connector. Verify that the display reads " 0.0000 " ±0.002.

g. Record results on operation verification test record, *Table 4-2.*

4-19. Voltmeter Verification

a. Proper operation will be checked by activating the voltage functions and verifying the correct display and LED indications.

b. Connect equipment as shown in *Figure 4-5.*

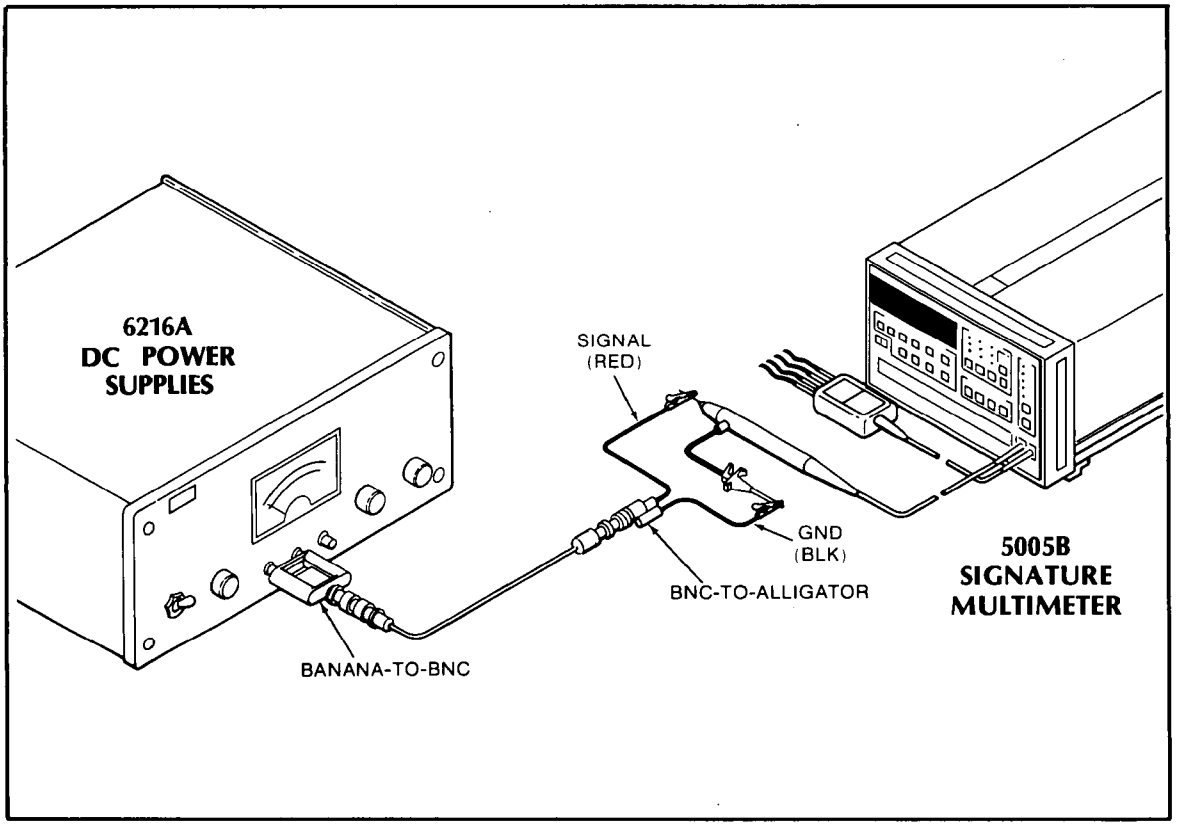


Figure 4-5. Voltmeter Operation Verification Test Setup

c. With the Data Probe tip grounded, press the 5005B front panel **DCV** pushbutton. Verify that the display reads " 0.000 " ±0.002.

d. With the Data Probe tip grounded, press the 5005B front panel **Vp+** pushbutton. Verify that the display reads " 0.00 " ±0.05 and the GATE light flashes.

e. With the Data Probe tip grounded, press the 5005B front panel **Vp–** pushbutton. Verify that the display reads " 0.00 " ±0.05.

f. With the **Vp–** function activated, connect the Data Probe tip to +5V on the 6216A Power Supply. Verify display reads " 5.00 " ±0.5.

NOTE

Perform the following tests with the Data Probe connected as in step f.

g. Press the 5005B front panel **Vp+** pushbutton. Verify that the display reads " 5.00 " ±0.5.

h. Press the 5005B front panel **ΔV** pushbutton. Verify that the display reads " 0.000 " ±0.5, and the PROBE SWITCH LED flashes. **Press the probe switch.**

i. Place the probe on Ground (⊥) and verify that the display reads " -5.00 " ±0.5.

j. Press the 5005B front panel **DCV** pushbutton. Verify that the display reads " 5.000 " ±0.300.

k. Record results on operation verification test record, *Table 4-2.*

4-20. Signature Analysis Verification

4-21. The following tests verify the signature analysis circuits of the 5005B. If a 5036A Microprocessor Lab is not available, any instrument with documented signature analysis capability can be used. Connect the 5005B Pod connectors as described in the substitute instrument's manual, and verify a documented signature. When using a substitute instrument for the 5036A, only the NORM mode of signature analysis can be verified unless the qualifier input is specified by the unit under test.

4-22. NORMAL Mode Verification

a. Proper operation will be checked by connecting the 5005B Signature Multimeter and 5036A Logic Lab and verifying correct signatures.

b. Set the 5005B LINE OFF-ON switch to ON. With the 5036 LINE switch "OFF", verify that four lighted bars are displayed, and the NORM key indicator, CLOCK, START, STOP rising edge, and all TTL level LED indicators are lighted. Verify that all other LEDs are unlighted.

c. Set the 5036A LINE OFF-ON switch to ON. Verify the ADDRESS/REGISTER and DATA LEDs read " 8888 88 " momentarily, then " uLAB UP ". Refer to *Figure 4-10.*

d. Set the 5036A LINE OFF-ON switch to OFF.

e. Set the 5036A switches as shown in *Figure 4-6.*

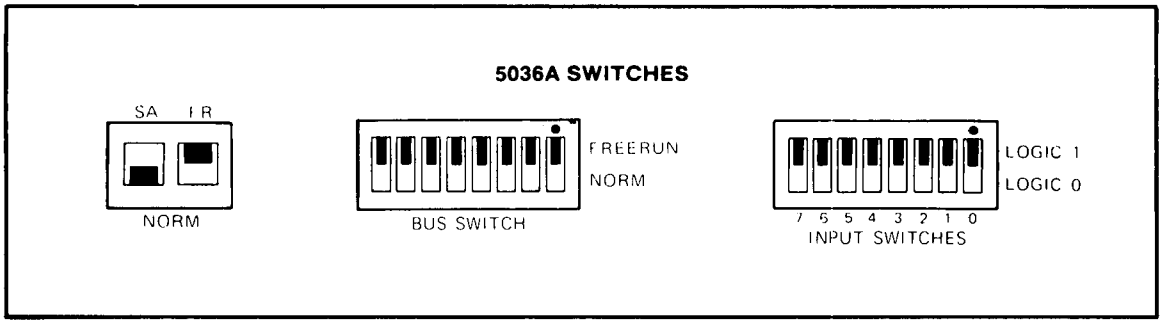


Figure 4-6. Signature Analysis, NORMAL Mode Switch Setting

f. Connect the 5005B to the 5036A as shown in *Figure 4-7.*

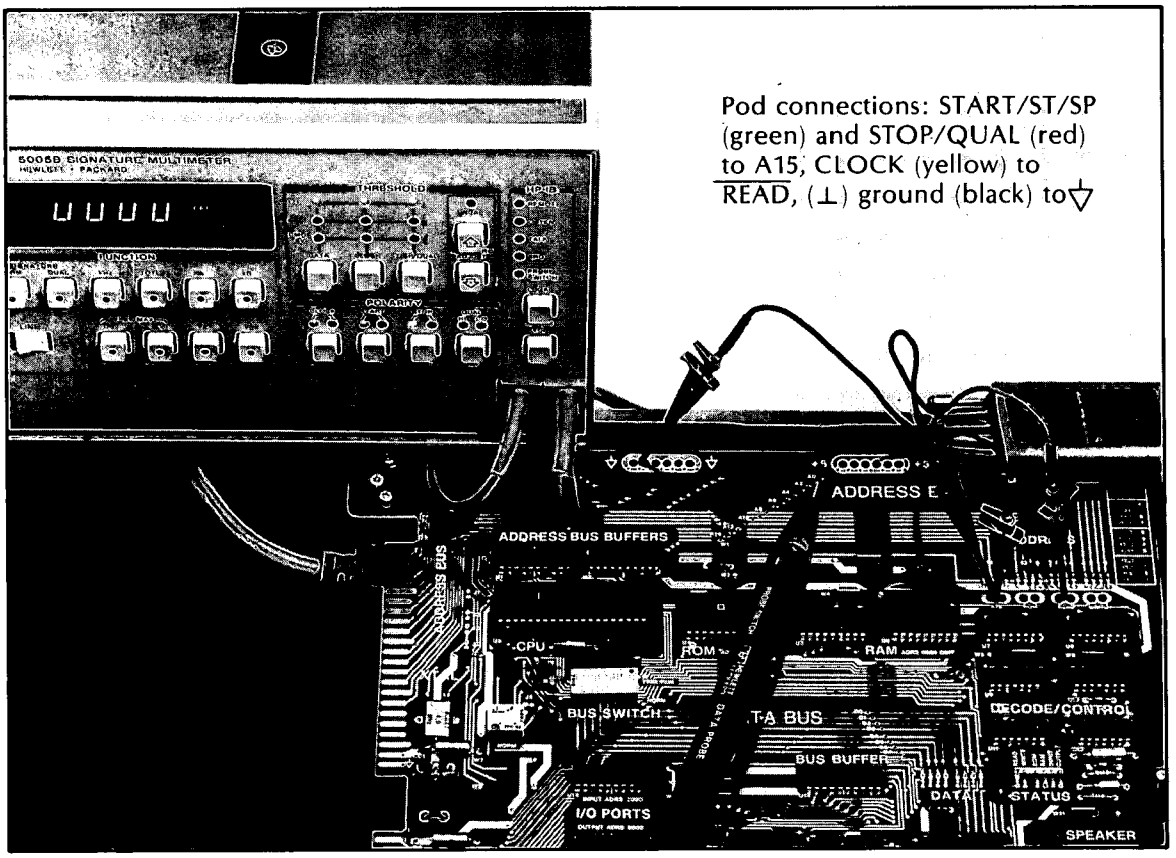


Figure 4-7. Signature Analysis, NORMAL Mode Operation Verification Test Setup

g. Set the 5036A LINE OFF-ON switch to ON. Verify the ADDRESS LEDs are lighted with the two leftmost LEDs blinking.

h. Connect the Data Probe to a +5 volt test connection (refer to *Figure 4-10*). Verify that the 5005B displays the signature " 0001 " with the GATE LED flashing and all other LED indications the same as in step b.

i. Connect the Data Probe to ADDRESS BUS test point A0 (refer to *Figure 4-10*). Verify that the 5005B displays the signature " UUUU " with the GATE LED flashing and all other LED indications are the same as in step b.

j. Set the 5005B and 5036A LINE OFF-ON switches to OFF, disconnect test equipment, and reconfigure the 5036A switches to their original positions. Record results on operation verification test record, *Table 4-2.*

4-23. QUAL Mode Verification

a. Proper operation will be checked by connecting the 5005B Signature Multimeter and 5036A Logic Lab and verifying correct signature indications.

b. Set the 5005B LINE OFF-ON switch to ON.

c. Set the 5036A LINE switch to "OFF". Press the 5005B (SIGNATURE) QUAL pushbutton. Press the POLARITY QUAL pushbutton (to toggle the qualifier to the low level position). Verify that four lighted bars are displayed, and the QUAL key indicator, CLOCK, START, STOP rising edge, QUAL falling edge, and all TTL level indicators are lighted. Verify that all other LEDs are unlighted.

d. Set the 5036A switches as shown in *Figure 4-8.*

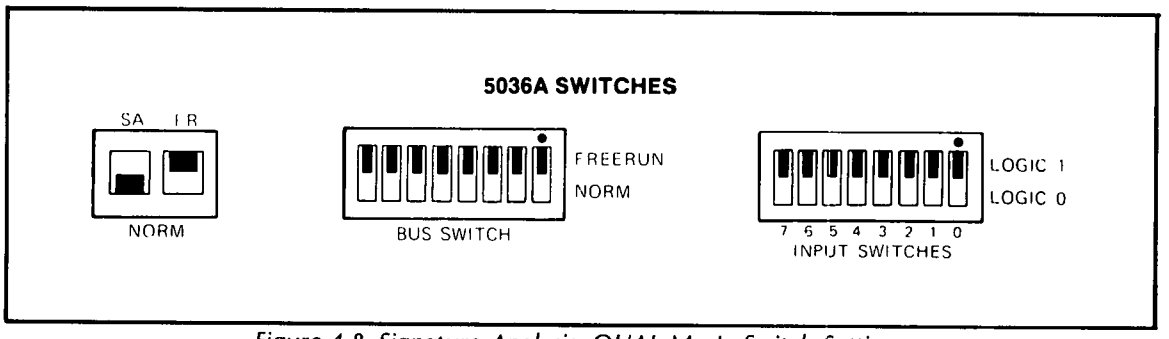


Figure 4-8. Signature Analysis, QUAL Mode Switch Settings

e. Connect the 5005B to the 5036A as shown in *Figure 4-9.*

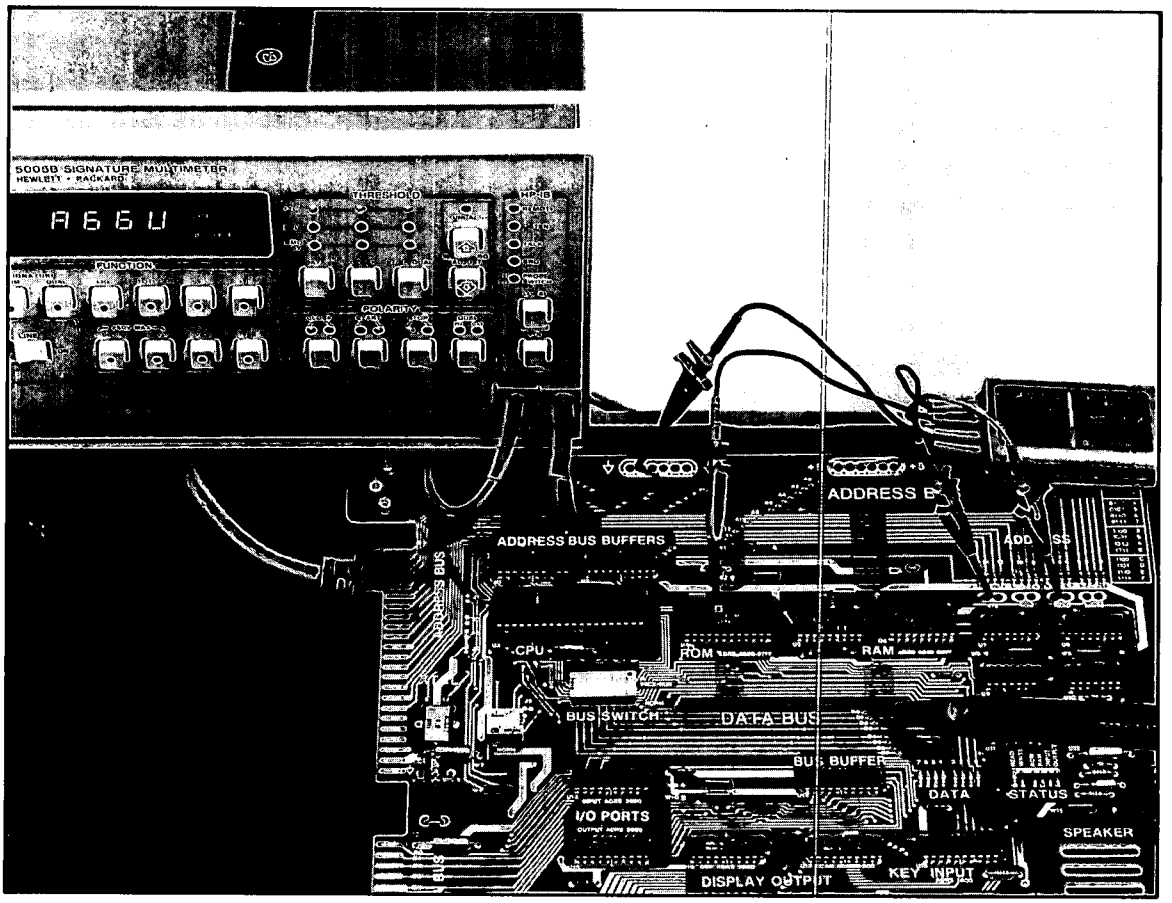


Figure 4-9. Signature Analysis QUAL Mode Operation Verification Test Setup

Pod connections: START/ST/SP (green) to A15
STOP/QUAL (red) to U4 pin 20
CLOCK (yellow) to $\overline{\text{READ}}$
(⊥) ground (black) to ⏚

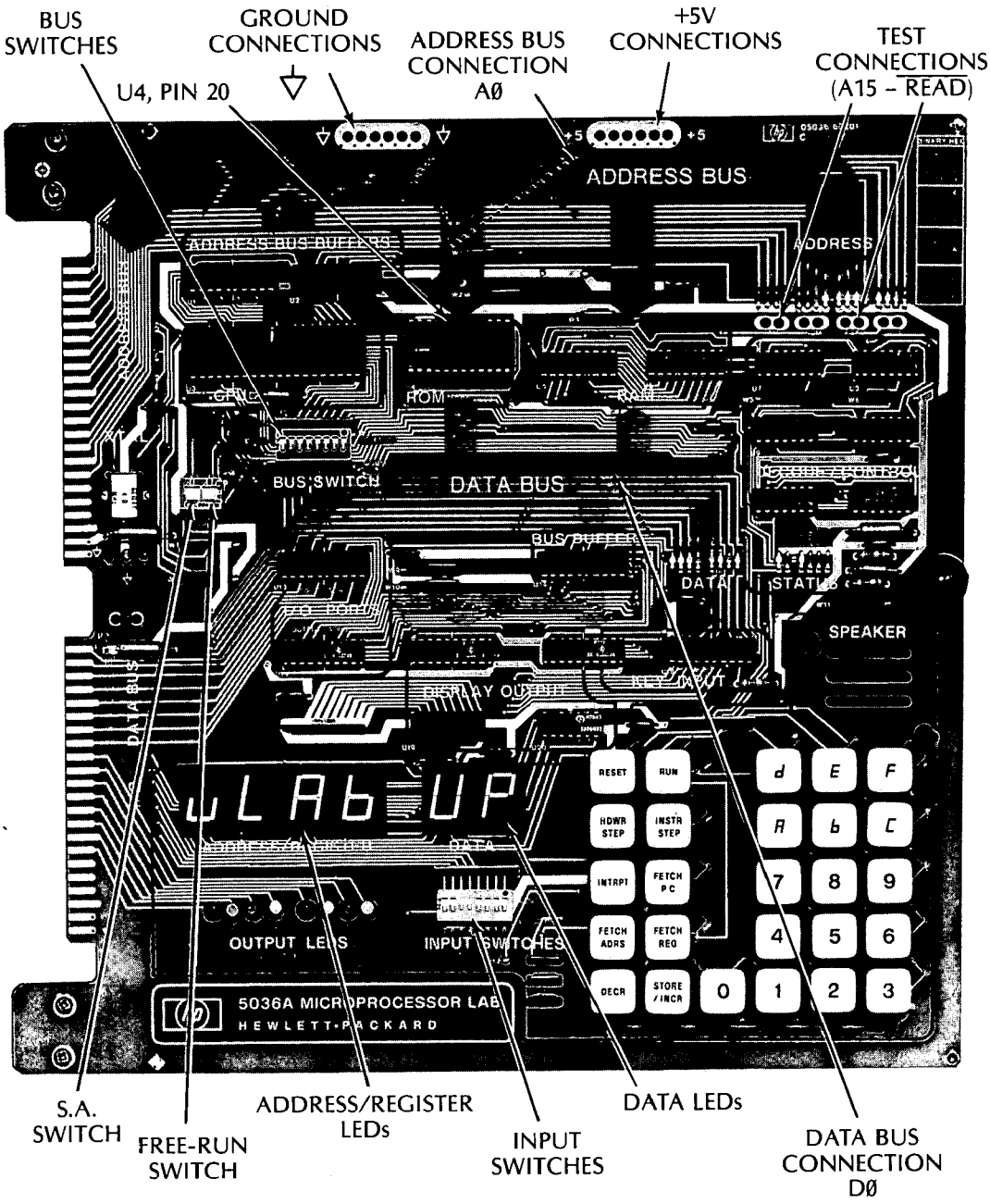


Figure 4-10. 5036A Test Switches and Connection Points

f. Set the 5036A LINE OFF-ON switch to ON. Verify the ADDRESS LEDs are lighted with the two leftmost LEDs blinking.

g. Connect the Data Probe to a +5 volt test connection (refer to *Figure 4-10*). Verify the 5005B displays the signature " 7870 " with the GATE LED flashing and all other LED indications the same as in step c.

h. Connect the Data Probe to DATA BUS test point D0 (refer to *Figure 4-10*). Verify that the 5005B display reads " A66U " with the GATE LED flashing and all other LED indications the same as in step c.

i. Set the 5005B and 5036A LINE OFF-ON switches to OFF, disconnect test equipment, and reconfigure the 5036A switches to their original positions. Record results on operation verification test record, *Table 4-2*.

4-24. HP-IB VERIFICATION

4-25. The HP 85A program listed in *Table 4-1* exercises the 5005B through the majority of its command code set via the HP-IB. If the 5005B successfully completes all checkpoints of the verification program, then there is a high probability that the HP-IB board (A8) and interface (A9) are functioning properly.

4-26. To perform the verification, set up the equipment as shown in *Figure 4-11*. Note that in addition to the HP 85A and the HP 5005B, the following equipment is required:

00085-15003	I/O ROM
82936A	ROM Drawer
82903A	16K Memory Module
82937A	HP-IB Interface Card/Cable

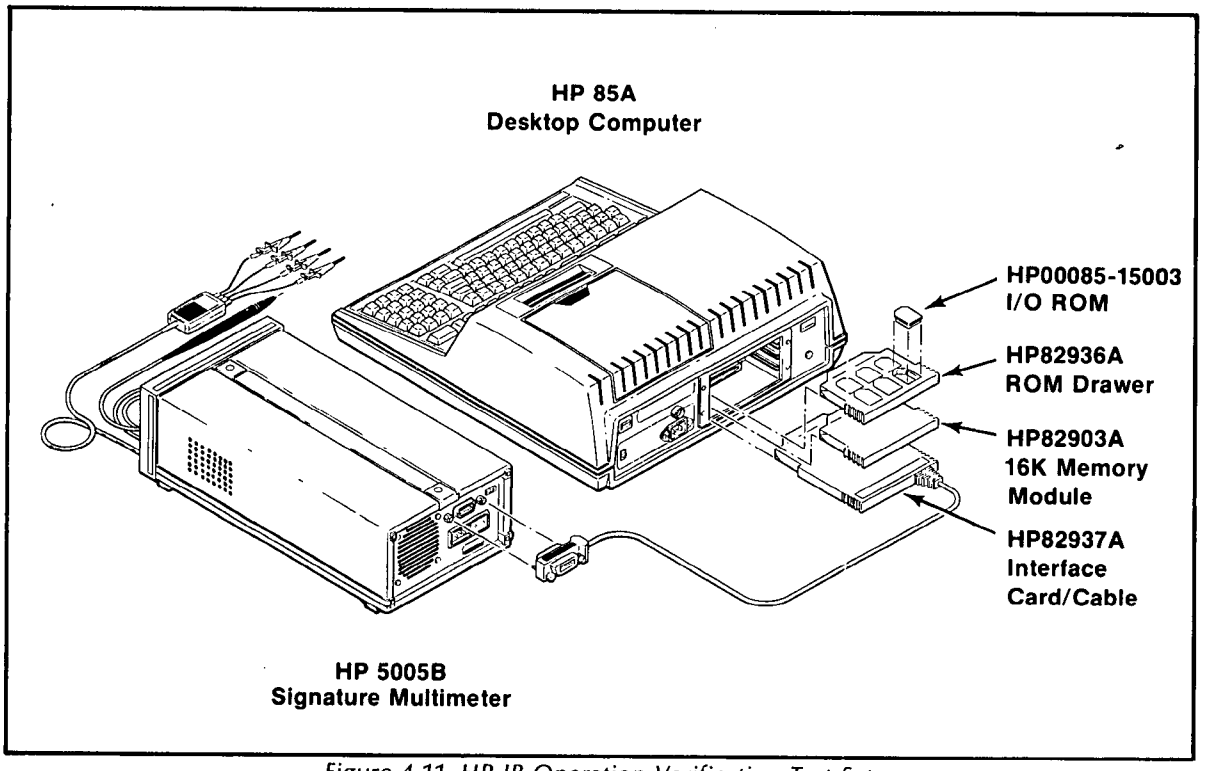


Figure 4-11. HP-IB Operation Verification Test Setup

4-27. The program listed in *Table 4-1* may be keyed into the HP 85A or loaded from an HP-IB Verification Cassette, HP P/N 59300-10002 Revision D (or later).

4-28. To run the program, insert the cassette in the HP 85A and power up the controller. If the controller power is already on, insert the cassette and type:

CHAIN "Autost"

then press END LINE.

4-29. Press the soft key corresponding to 5005B, and follow the instructions shown on the HP 85A screen.

4-30. The program automatically starts and displays the program title, then the following checkpoint summary

```
**********************************

        CHECKPOINT SUMMARY

**********************************

 1  Power-up Preset
 2  Remote, Local, Local Lockout
 3  Function Select
 4  Polarity Select
 5  Threshold Select
 6  Uncal Threshold Settings
 7  Reset
 8  Reading Panel Setup
 9  Reading Threshold Values
10  Probe Switch Enable
11  Service Request
12  Status Byte
13  Send Error Code
14  Alarm
```

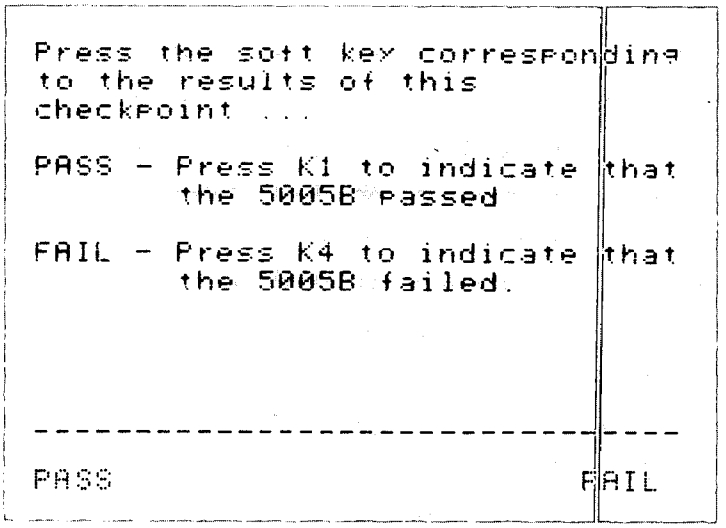
4-31. The next screen provides the option to receive a printed version of this summary.

4-32. Equipment set up instructions are provided (with reference made to the manual), then the HP 85A searches for the address of the 5005B. This search eliminates the need to set the 5005B rear panel address switches and thus, allows an arbitrary address setting. If the address is not found, one or more of the following may be the cause:

HP5005B	— not powered up — in TALK ONLY mode
Interface	— not connected — defective
Address of 5005B	— set to 721 (calculator address) — set to 731

4-33. After these initial steps, the program begins the checkpoint execution. The HP 85A display provides the description and operator instructions as each checkpoint is performed.

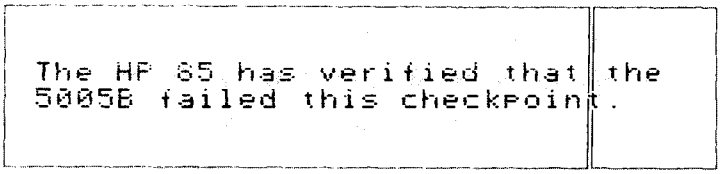
4-34. At the end of most of the checkpoints, the HP 85A displays the following prompt:



4-35. As instructed, press the soft key corresponding to the checkpoint results.

4-36. For checkpoints 8, 9, 12, and 13, one of the following messages will be displayed instead of the above message:

or



4-37. As indicated, the HP 85A has been instructed to verify the results of the checkpoint and display its decision.

4-38. The next screen displayed by the HP 85A is shown below:

```
Press a soft key to select the
desired checkpoint ...

NEXT -    Press K1 to perform the
          next checkpoint.

REPEAT -  Press K3 to repeat this
          checkpoint.

GOTO# -   Press K4 to select an
          arbitrary checkpoint.

--------------------------------

NEXT                  REPEAT  GOTO#
```

4-39. The format of the program allows the user to proceed in a sequential order to the next checkpoint, repeat the present checkpoint, or go to an arbitrary checkpoint.

4-40. When "GO TO #" has been selected, the following prompt occurs:

```
Enter checkpoint number desired
(0 to 14), and press END LINE
(0 TERMINATES PROGRAM).
?
```

4-41. Entering a number other than 0 causes that checkpoint number to be executed. If 0 is entered, the program terminates by displaying the checkpoint results, and providing the option to receive a printed version. An example of the printed checkpoint results is shown below:

```
**********************************

      CHECKPOINT RESULTS
    FOR HP-IB ADDRESS 703

**********************************

CHECKPOINT   1  PASS
             2  PASS
             3  PASS
             4  FAIL
             5  NOT PERFORMED
             6  PASS
             7  PASS
             8  NOT PERFORMED
             9  PASS
             10 FAIL
             11 NOT PERFORMED
             12 NOT PERFORMED
             13 PASS
             14 FAIL
```

NOTE

The 5005B front panel local key may be pressed between, but not during, any checkpoint.

Table 4-1. HP-IB Operation Verification Program Listing

```
10 ! ******* HP 5005B *******
20 !      HP-IB OPERATION
30 !    VERIFICATION PROGRAM
40 !
50 !  KBC
60 !  DATE : 7 April 1982
70 !  REVISION A
80 !
90 ! This program exercises the 5005B through the majority
100 ! of its command code set via HP-IB. The program consists
110 ! of 14 checkpoints, and provides the user with the ability
120 ! to execute and repeat these tests in any order.
130 ! Also provided are options to print the checkpoint
140 ! summary and results. The program relies heavily on
150 ! subroutines in addition to arrays and simple variables.
160 !
170 ! VARIABLE TABLE
180 !    A     (Address)
190 !    B     (Byte information)
200 !    C     (CRT status)
210 !    D     (Decision)
220 !    E     (Error value)
230 !    I     (Loop variable)
240 !    L     (CLOCK uncal value)
250 !    M     (S/S/Q uncal value)
260 !    R     (Result variable)
270 !    R()   (Result array)
280 !    S     (Step number)
290 !    V     (Value of byte)
300 !
310 NORMAL
320 ! DIMENSION AND INITIALIZE STRING VARIABLE ARRAYS
330 DIM A$[30],B$[30],C$[30],D$[30],E$[30],F$[30],G$[30],H$[35]
340 DIM I$[35],J$[10],K$[10],L$[15],M$[15],N$[10],R(14)
350 A$="Press CONT to perform test."
360 B$="Press CONT when ready."
370 C$="Verify that 5005B front panel"
380 D$="Verify that 5005B display"
390 E$="After pressing CONT, "
400 F$="Press CONT for next display."
410 G$="           CHECKPOINT "
420 H$="********************************"
430 !
440 FOR I=1 TO 14
450 R(I)=0
460 NEXT I
470 CRT IS 1 @ C=1
480 ENABLE KBD 1+32
490 !
500 ! DISPLAY TITLE, CHECKPOINT LIST AND SETUP INSTRUCTIONS
510 BEEP @ CLEAR @ DISP USING "5/"
520 DISP H$ @ DISP
530 DISP "      5005B HP-IB OPERATION"
540 DISP "      VERIFICATION PROGRAM"
550 DISP @ DISP H$ @ DISP
560 WAIT 2500
570 CLEAR @ DISP USING "5/"
580 DISP H$ @ DISP
590 DISP "        CHECKPOINT SUMMARY"
600 DISP @ DISP H$ @ DISP
610 IF C=2 THEN 630
620 WAIT 2000 @ CLEAR
630 DISP " 1  Power-up Preset"
640 DISP " 2  Remote, Local, Local Lockout"
650 DISP " 3  Function Select"
660 DISP " 4  Polarity Select"
```

Table 4-1. HP-IB Operation Verification Program Listing (Continued)

```
670 DISP " 5  Threshold Select"
680 DISP " 6  Uncal Threshold Settings"
690 DISP " 7  Reset"
700 DISP " 8  Reading Panel Setup"
710 DISP " 9  Reading Threshold Values"
720 DISP "10  Probe Switch Enable"
730 DISP "11  Service Request"
740 DISP "12  Status Byte"
750 DISP "13  Send Error Code"
760 DISP "14  Alarm"
770 IF C=2 THEN DISP USING "5/" @ GOTO 890
780 DISP USING "#,K,/" ; F$ @ PAUSE
790 CLEAR
800 DISP "Would you like a printed versionof the checkpoint summary?"
810 DISP @ DISP "YES - Press K1 to receive a           printed version."
820 DISP @ DISP "NO -  Press K4 to proceed."
830 ON KEY# 1,"YES" GOTO 870
840 ON KEY# 4,"    NO" GOTO 900
850 KEY LABEL
860 GOTO 860
870 CLEAR @ CRT IS 2 @ C=2
880 GOTO 580
890 CRT IS 1 @ C=1
900 CLEAR
910 DISP "The HP 85 should have an I/O ROMin its ROM Drawer, a 16K"
920 DISP "Memory Module, and an 82937A    HP-IB Interface Card/Cable."
930 DISP "Connect the HP-IB Interface to  the rear panel of the HP 5005B"
940 DISP "and power-up the instrument."
950 DISP @ DISP "Consult the HP 5005B Operating  and Programming Manual for"
960 DISP "additional information."
970 DISP @ DISP B$ @ PAUSE
980 !
990 ! SEARCH FOR 5005B ADDRESS
1000 CLEAR @ DISP "Searching for 5005B address..."
1010 N$="NOT5005B"
1020 SET TIMEOUT 7;100
1030 FOR A=700 TO 730
1040 IF A=721 THEN 1110
1050 REMOTE A
1060 OUTPUT A ;"ID"
1070 ENTER A ; N$
1080 IF N$="HP5005B" THEN 1180
1090 CLEAR A
1100 ABORTIO 7
1110 NEXT A
1120 BEEP @ WAIT 250 @ BEEP
1130 DISP @ DISP "Address not found."
1140 DISP @ DISP "Verify HP-IB connection, and    that the 5005B is powered up"
1150 DISP "and not in the TALK ONLY mode."
1160 DISP @ DISP B$ @ PAUSE
1170 GOTO 1000
1180 DISP @ DISP "HP 5005B found at address";A;"." @ WAIT 2000
1190 SET TIMEOUT 7;0
1200 !
1210 ! CHECKPOINT 1
1220 I$="          Power-up Preset"
1230 S=1 @ GOSUB 4710
1240 DISP "Toggle the 5005B line switch    from ON to OFF, then back to ON."
1250 DISP @ DISP "Verify that the 5005B sounds an audible tone."
1260 DISP @ DISP F$ @ PAUSE
1270 CLEAR @ DISP C$
1280 DISP "NORM SIGNATURE annunciator is   lit, the CLOCK, START, and STOP"
1290 DISP "polarities are set to the risingedge, and DATA, CLOCK, and "
1300 DISP "ST/SP/QUAL thresholds are set toTTL levels."
1310 DISP @ DISP D$;" shows"
1320 DISP "/  ----/."
```

Table 4-1. HP-IB Operation Verification Program Listing (Continued)

```
1330 DISP @ DISP USING "#,K,/" ; F$ @ PAUSE
1340 GOTO 4860
1350 !
1360 ! CHECKPOINT 2
1370 I$="  Remote, Local, Local Lockout"
1380 S=2 @ GOSUB 4710
1390 LOCAL 7 @ ABORTIO 7
1400 DISP E$;"the 5005B" @ DISP "will be placed under remote     control."
1410 GOSUB 5290
1420 REMOTE A
1430 CLEAR @ DISP "Verify that the REMOTE and      LISTEN status LEDs are lit."
1440 DISP @ DISP F$ @ PAUSE
1450 CLEAR @ DISP E$;"the 5005B"
1460 DISP "will be placed in the LOCAL     LOCKOUT mode."
1470 GOSUB 5290
1480 LOCAL LOCKOUT 7
1490 CLEAR
1500 DISP "Press the front panel LOCAL key to verify that the 5005B is in"
1510 DISP "LOCAL LOCKOUT and remains in    REMOTE."
1520 DISP @ DISP F$ @ PAUSE
1530 CLEAR @ DISP E$;"the 5005B"
1540 DISP "will be placed in the LOCAL     mode."
1550 GOSUB 5290
1560 LOCAL 7
1570 CLEAR @ DISP C$
1580 DISP "REMOTE status LED is now unlit."
1590 GOTO 4810
1600 !
1610 ! CHECKPOINT 3
1620 I$="          Function Select"
1630 S=3 @ GOSUB 4710
1640 DISP E$;"verify that"
1650 DISP "the FUNCTION key button          annunciators light in sequence "
1660 DISP "from NORM(F0) to Vp-(F9), and   back to NORM. A tone will sound"
1670 DISP "to mark each function change."
1680 DISP @ DISP USING "#,K,/" ; A$ @ PAUSE
1690 REMOTE A
1700 OUTPUT A ;"F0" @ WAIT 1000
1710 OUTPUT A ;"F1" @ GOSUB 5350
1720 OUTPUT A ;"F2" @ GOSUB 5350
1730 OUTPUT A ;"F3" @ GOSUB 5350
1740 OUTPUT A ;"F4" @ GOSUB 5350
1750 OUTPUT A ;"F5" @ GOSUB 5350
1760 OUTPUT A ;"F6" @ GOSUB 5350
1770 OUTPUT A ;"F7" @ GOSUB 5350
1780 OUTPUT A ;"F8" @ GOSUB 5350
1790 OUTPUT A ;"F9" @ GOSUB 5350
1800 OUTPUT A ;"F0" @ GOSUB 5350
1810 GOTO 4860
1820 !
1830 ! CHECKPOINT 4
1840 I$="          Polarity Select"
1850 S=4 @ GOSUB 4710
1860 DISP E$;"verify that"
1870 DISP "the trigger edge of the CLOCK,"
1880 DISP "START, STOP, and QUAL polarities(in that order) toggles."
1890 DISP "A tone will sound to mark each  polarity change."
1900 DISP @ DISP USING "#,K,/" ; A$ @ PAUSE
1910 REMOTE A
1920 OUTPUT A ;"F1 PC1 PT1 PP1 PQ1" @ WAIT 1000
1930 OUTPUT A ;"PC2" @ GOSUB 5350
1940 OUTPUT A ;"PC1" @ GOSUB 5350
1950 OUTPUT A ;"PT2" @ GOSUB 5350
1960 OUTPUT A ;"PT1" @ GOSUB 5350
1970 OUTPUT A ;"PP2" @ GOSUB 5350
1980 OUTPUT A ;"PP1" @ GOSUB 5350
```

Table 4-1. HP-IB Operation Verification Program Listing (Continued)

```
1990 OUTPUT A ;"PQ2" @ GOSUB 5350
2000 OUTPUT A ;"PQ1" @ GOSUB 5350
2010 GOTO 4860
2020 !
2030 ! CHECKPOINT 5
2040 I$="         Threshold Select"
2050 S=5 @ GOSUB 4710
2060 DISP E$;"verify that"
2070 DISP "the threshold select scans down through the three logic families"
2080 DISP "for the DATA, CLOCK, then       ST/SP/QUAL parameters."
2090 DISP @ DISP F$ @ PAUSE
2100 CLEAR @ DISP "A tone will sound to mark each  threshold change."
2110 GOSUB 5290
2120 REMOTE A
2130 OUTPUT A ;"F1 TD1 TC1 TQ1" @ WAIT 1000
2140 OUTPUT A ;"TD2" @ GOSUB 5350
2150 OUTPUT A ;"TD3" @ GOSUB 5350
2160 OUTPUT A ;"TD1" @ GOSUB 5350
2170 OUTPUT A ;"TC2" @ GOSUB 5350
2180 OUTPUT A ;"TC3" @ GOSUB 5350
2190 OUTPUT A ;"TC1" @ GOSUB 5350
2200 OUTPUT A ;"TQ2" @ GOSUB 5350
2210 OUTPUT A ;"TQ3" @ GOSUB 5350
2220 OUTPUT A ;"TQ1" @ GOSUB 5350
2230 GOTO 4860
2240 !
2250 ! CHECKPOINT 6
2260 I$="Uncalibrated Threshold Settings"
2270 S=6 @ GOSUB 4710
2280 J$="2.10H" @ K$="0.70L" @ L=1.55 @ M=1.35
2290 DISP E$;"the 5005B "
2300 DISP "will be programmed to these     uncalibrated levels for TTL"
2310 DISP "logic:"
2320 GOSUB 5400
2330 REMOTE A
2340 OUTPUT A ;"UD1 H2.10 L0.70 UC1 1.55 UQ1 1.35"
2350 CLEAR @ DISP C$
2360 DISP "UNCAL LED is lit." @ DISP
2370 GOSUB 5470
2380 J$="-1.00H" @ K$="-1.60L" @ L=-1.25 @ M=-1.45
2390 CLEAR @ DISP E$;"the 5005B"
2400 DISP "will be programmed to these     uncalibrated levels for ECL"
2410 DISP "logic:"
2420 GOSUB 5400
2430 OUTPUT A ;"UD2 H-1.00 L-1.60  UC2 -1.25 UQ2 -1.45"
2440 CLEAR @ DISP C$
2450 DISP "UNCAL LED remains lit." @ DISP
2460 GOSUB 5470
2470 J$="3.60H" @ K$="1.40L" @ L=2.45 @ M=2.55
2480 CLEAR @ DISP E$;"the 5005B"
2490 DISP "will be programmed to these     uncalibrated levels for 5V CMOS"
2500 DISP "logic:"
2510 GOSUB 5400
2520 OUTPUT A ;"UD3 H3.60 L1.40 UC3 2.45 UQ3 2.55"
2530 CLEAR @ DISP C$
2540 DISP "UNCAL LED remains lit." @ DISP
2550 GOSUB 5470 @ GOTO 4860
2560 !
2570 ! CHECKPOINT 7
2580 I$="              RESET"
2590 S=7 @ GOSUB 4710
2600 DISP E$;"the 5005B"
2610 DISP "will be reset to its power-up   conditions."
2620 GOSUB 5290
2630 REMOTE A
2640 OUTPUT A ;"RS" @ WAIT 2000
```

Table 4-1. HP-IB Operation Verification Program Listing (Continued)

```
2650 CLEAR @ DISP C$
2660 DISP "NORM SIGNATURE annunciator is   lit, CLOCK, START, and STOP"
2670 DISP "polarities are set to the risingedge, DATA, CLOCK, and"
2680 DISP "ST/SP/QUAL thresholds are set toTTL levels, and the REMOTE and"
2690 DISP "LISTEN status LEDs are lit."
2700 DISP @ DISP D$
2710 DISP "shows ´  ----´"
2720 GOTO 4810
2730 !
2740 ! CHECKPOINT 8
2750 I$="       Reading Panel Setup"
2760 S=8 @ GOSUB 4710
2770 R=1
2780 DISP E$;"the 5005B"
2790 DISP "will be reset, and the front    panel setup will be read by the"
2800 DISP "controller."
2810 GOSUB 5290
2820 REMOTE A
2830 OUTPUT A ;"RSSU"
2840 CLEAR
2850 DISP "Six bytes of binary coded       information have been read. The"
2860 DISP "first contains information aboutthe function setting."
2870 V=0 @ GOSUB 5590
2880 CLEAR
2890 DISP "The second byte contains        information about the polarity"
2900 DISP "settings."
2910 V=21 @ GOSUB 5590
2920 CLEAR
2930 DISP "The third byte contains         information about the threshold"
2940 DISP "settings."
2950 V=21 @ GOSUB 5590
2960 CLEAR
2970 DISP "The fourth byte contains        information about the SRQ mask."
2980 V=0 @ GOSUB 5590
2990 CLEAR @ DISP "The fifth byte contains the     carriage return information."
3000 V=13 @ GOSUB 5590
3010 CLEAR @ DISP "The sixth byte contains the linefeed information."
3020 V=10 @ GOSUB 5590
3030 GOSUB 5970 @ GOTO 4870
3040 !
3050 ! CHECKPOINT 9
3060 I$="    Reading Threshold Values"
3070 S=9 @ GOSUB 4710
3080 R=1
3090 DISP E$;"the 5005B" @ DISP "will be reset, and the DATA "
3100 GOSUB 5740
3110 REMOTE A
3120 OUTPUT A ;"RSTH1"
3130 L$="H+02.00 L+00.80"
3140 GOSUB 5800
3150 CLEAR @ DISP E$;"the CLOCK"
3160 GOSUB 5740
3170 OUTPUT A ;"TH2"
3180 L$="+01.40 "
3190 GOSUB 5800
3200 CLEAR @ DISP E$;"ST/SP/QUAL"
3210 GOSUB 5740
3220 OUTPUT A ;"TH3"
3230 L$="+01.40 "
3240 GOSUB 5800 @ GOSUB 5970 @ GOTO 4870
3250 !
3260 ! CHECKPOINT 10
3270 I$="       Probe Switch Enable"
3280 S=10 @ GOSUB 4710
3290 DISP E$;"verify"
3300 DISP "that the front panel PROBE      SWITCH status LED flashes for 5"
```

Table 4-1. HP-IB Operation Verification Program Listing (Continued)

```
3310 DISP "seconds, then goes out."
3320 DISP "A tone will mark each probe     switch state change."
3330 DISP @ DISP USING "#,K,/" ; A$ @ PAUSE
3340 REMOTE A
3350 OUTPUT A ;"PS1"
3360 BEEP @ WAIT 5000
3370 OUTPUT A ;"PS0" @ BEEP
3380 GOTO 4860
3390 !
3400 ! CHECKPOINT 11
3410 I$="          Service Request"
3420 S=11 @ GOSUB 4710
3430 DISP E$;"the probe"
3440 DISP "switch will be enabled, and the service request mask will be set"
3450 DISP "to generate an SRQ on a probe   switch press."
3460 DISP @ DISP USING "#,K,/" ; A$ @ PAUSE
3470 REMOTE A
3480 OUTPUT A ;"QM2PS1"
3490 CLEAR @ DISP "Now press the probe switch to   generate the SRQ."
3500 DISP @ DISP C$
3510 DISP "PROBE SWITCH LED stops flashing and remains lit, and the SRQ "
3520 DISP "status LED lights after the     probe switch press."
3530 DISP @ DISP F$ @ PAUSE
3540 CLEAR @ DISP E$;"the" @ DISP "service request mask will be "
3550 DISP "cleared, but the probe switch   will remain enabled."
3560 GOSUB 5290
3570 B=SPOLL(A)
3580 OUTPUT A ;"QM0PS1"
3590 CLEAR
3600 DISP "Now press the probe switch and  verify that no SRQ is generated."
3610 DISP
3620 DISP "The PROBE SWITCH LED will stop  flashing and remain lit to "
3630 DISP "indicate a probe switch press."
3640 DISP @ DISP F$ @ PAUSE
3650 OUTPUT A ;"PS0"
3660 GOTO 4860
3670 !
3680 ! CHECKPOINT 12
3690 I$="            Status Byte"
3700 S=12 @ GOSUB 4710
3710 R=1
3720 DISP E$;"the 5005B"
3730 DISP "will be reset, and the status   byte will be read by the"
3740 DISP "controller."
3750 GOSUB 5290
3760 REMOTE A
3770 OUTPUT A ;"RS"
3780 B=SPOLL(A)
3790 ! READ STATUS UNTIL 5005B HAS FINISHED RESET EXECUTION
3800 IF B=40 THEN 3780
3810 CLEAR @ DISP "The correct value for the statusbyte after reset is 32 ."
3820 DISP @ DISP "The returned value of the statusbyte is";B;"."
3830 IF B=32 THEN R=R*1
3840 IF B<>32 THEN R=R*0
3850 DISP @ DISP F$ @ PAUSE
3860 GOSUB 5970 @ GOTO 4870
3870 !
3880 ! CHECKPOINT 13
3890 I$="          Send Error Code"
3900 S=13 @ GOSUB 4710
3910 R=1
3920 DISP E$;"an"
3930 DISP "unrecognizable command code willbe sent to the 5005B to generate"
3940 DISP "an error."
3950 GOSUB 5290
3960 REMOTE A
```

Table 4-1. HP-IB Operation Verification Program Listing (Continued)

```
3970 OUTPUT A ;"ILLEGAL COMMAND"
3980 CLEAR
3990 DISP "Verify that the 5005B sounds    audible beeps and the display"
4000 DISP "shows ' Err15'."
4010 DISP @ DISP E$;"the error"
4020 DISP "for this illegal command will besent to the controller."
4030 GOSUB 5290
4040 LOCAL 7
4050 WAIT 3000
4060 E=0
4070 CLEAR @ DISP "The expected value for this     error code is 82 ."
4080 REMOTE A
4090 OUTPUT A ;"SE"
4100 ENTER A ; E
4110 DISP @ DISP "The returned value for this     error code is ";E;"."
4120 IF E=82 THEN R=R*1
4130 IF E<>82 THEN R=R*0
4140 DISP @ DISP F$ @ PAUSE
4150 GOSUB 5970 @ GOTO 4870
4160 !
4170 ! CHECKPOINT 14
4180 I$="               Alarm"
4190 S=14 @ GOSUB 4710
4200 DISP E$;"the 5005B"
4210 DISP "will be programmed to sound the alarm once, three times, then "
4220 DISP "ten times. A tone by the        controller will mark each"
4230 DISP "transition."
4240 DISP @ DISP USING "#,K,/" ; A$ @ PAUSE
4250 GOSUB 5350
4260 REMOTE A
4270 OUTPUT A ;"AL1" @ WAIT 1000
4280 GOSUB 5350
4290 OUTPUT A ;"AL2" @ WAIT 1500
4300 GOSUB 5350
4310 OUTPUT A ;"AL3" @ WAIT 3000
4320 GOTO 4860
4330 !
4340 ! END OF PROGRAM
4350 CLEAR @ DISP H$
4360 DISP @ DISP "       CHECKPOINT RESULTS"
4370 DISP "     FOR HP-IB ADDRESS";A
4380 DISP @ DISP H$
4390 IF C=2 THEN DISP @ GOTO 4410
4400 DISP @ DISP F$ @ PAUSE
4410 CLEAR
4420 FOR I=1 TO 14
4430 IF R(I)=0 THEN R$="NOT PERFORMED"
4440 IF R(I)=1 THEN R$="FAIL"
4450 IF R(I)=2 THEN R$="PASS"
4460 IF I=1 THEN DISP "CHECKPOINT ";I;" ";R$ @ GOTO 4490
4470 IF I<10 THEN DISP "            ";I;" ";R$ @ GOTO 4490
4480 DISP "           ";I;R$
4490 NEXT I
4500 IF C=2 THEN DISP USING "5/" @ GOTO 4620
4510 DISP USING "#,K,/" ; F$ @ PAUSE
4520 CLEAR @ DISP "Would you like a printed versionof the checkpoint results?"
4530 DISP @ DISP "YES - Press K1 to receive a           printed version."
4540 DISP @ DISP "NO -  Press K4 to proceed."
4550 ON KEY# 1,"YES" GOTO 4600
4560 OFF KEY# 3
4570 ON KEY# 4,"     NO" GOTO 4630
4580 KEY LABEL
4590 GOTO 4590
4600 CLEAR @ CRT IS 2 @ C=2
4610 GOTO 4350
4620 CRT IS 1 @ C=1
```

Table 4-1. HP-IB Operation Verification Program Listing (Continued)

```
4630 LOCAL 7 @ ABORTIO 7 @ REWIND
4640 CLEAR @ DISP USING "5/"
4650 DISP H$ @ DISP
4660 DISP "END OF HP 5005B HP-IB OPERATION      VERIFICATION PROGRAM"
4670 DISP @ DISP H$
4680 END
4690 !
4700 !
4710 ! SUBROUTINE TO PRINT CHECKPOINT HEADINGS
4720 CLEAR
4730 DISP H$
4740 DISP
4750 DISP G$;S
4760 DISP I$
4770 DISP
4780 DISP H$
4790 DISP
4800 RETURN
4810 !
4820 ! SUBPROGRAM TO TERMINATE CHECKPOINT EXECUTION
4830 DISP
4840 DISP F$
4850 PAUSE
4860 GOSUB 4890
4870 GOSUB 5030
4880 GOTO 5230
4890 !
4900 ! SUBROUTINE TO PROMPT USERFOR CHECKPOINT RESULTS
4910 CLEAR
4920 DISP "Press the soft key correspondingto the results of this"
4930 DISP "checkpoint ... "
4940 DISP @ DISP "PASS - Press K1 to indicate that       the 5005B passed."
4950 DISP @ DISP "FAIL - Press K4 to indicate that       the 5005B failed."
4960 ON KEY# 1,"PASS" GOTO 5010
4970 OFF KEY# 3
4980 ON KEY# 4,"   FAIL" GOTO 5020
4990 KEY LABEL
5000 GOTO 5000
5010 R(S)=2 @ RETURN
5020 R(S)=1 @ RETURN
5030 !
5040 ! SUBROUTINE TO DETERMINE NEXT PROGRAM STEP
5050 CLEAR
5060 DISP "Press a soft key to select the  desired checkpoint ..."
5070 DISP @ DISP "NEXT -   Press K1 to perform the         next checkpoint."
5080 DISP @ DISP "REPEAT - Press K3 to repeat this         checkpoint."
5090 DISP
5100 DISP "GOTO# -  Press K4 to select an           arbitrary checkpoint."
5110 ON KEY# 1,"NEXT" GOTO 5160
5120 ON KEY# 3,"  REPEAT" GOTO 5170
5130 ON KEY# 4,"  GOTO#" GOTO 5180
5140 KEY LABEL
5150 GOTO 5150
5160 D=S+1 @ RETURN
5170 D=S @ RETURN
5180 CLEAR
5190 DISP "Enter checkpoint number desired (0 to 14), and press END LINE"
5200 DISP "(0 TERMINATES PROGRAM)." @ INPUT D
5210 IF D<0 OR D>14 THEN 5180
5220 RETURN
5230 !
5240 ! SUBPROGRAM TO BRANCH EXECUTION TO DESIRED CHECKPOINT
5250 IF D=0 THEN 4330
5260 IF D>7 THEN 5280
5270 ON D GOTO 1200,1350,1600,1820,2020,2240,2560
5280 ON D-7 GOTO 2730,3040,3250,3390,3670,3870,4160,4330
```

Table 4-1. HP-IB Operation Verification Program Listing (Continued)

```
5290 !
5300 ! SUBROUTINE TO PROMT USER AND PAUSE
5310 DISP
5320 DISP A$
5330 PAUSE
5340 RETURN
5350 !
5360 ! SUBROUTINE TO BEEP AND WAIT 1.5 SECONDS
5370 BEEP 250,20
5380 WAIT 1500
5390 RETURN
5400 !
5410 ! SUBROUTINE FOR CHECKPOINT 6 DISPLAY
5420 DISP "DATA:         H=";J$;"   L=";K$
5430 DISP "CLOCK:       ";L
5440 DISP "ST/SP/QUAL: ";M
5450 DISP USING "#,K,/" ; A$ @ PAUSE
5460 RETURN
5470 !
5480 ! SUBROUTINE TO INSTRUCT USER TO RECALL UNCALIBRATED
5490 ! THRESHOLD VALUES FROM 5005B FRONT PANEL
5500 LOCAL 7
5510 DISP "To verify uncalibrated settings,press:"
5520 DISP "DATA key:  once to view ";J$
5530 DISP "           again to view ";K$
5540 DISP "CLOCK key  to view ";L
5550 DISP "ST/SP/QUAL key to view ";M
5560 DISP @ DISP F$ @ PAUSE
5570 REMOTE A
5580 RETURN
5590 !
5600 ! SUBROUTINE TO PROMPT USER AND READ A PANEL SETUP BYTE
5610 DISP @ DISP E$;"this byte"
5620 DISP "will be available for viewing."
5630 GOSUB 5290
5640 B=1
5650 ENTER A USING "#,B" ; B
5660 DISP "The correct value is ";V;"."
5670 DISP "The returned value for this byteis ";B;"."
5680 IF B=V THEN R=R*1
5690 IF B<>V THEN R=R*0
5700 DISP
5710 DISP USING "#,K,/" ; F$
5720 PAUSE
5730 RETURN
5740 !
5750 ! SUBROUTINE TO DISPLAY MESSAGE AND PROMPT USER
5760 DISP "threshold values for the currentthreshold settings will be read"
5770 DISP "by the controller."
5780 GOSUB 5290
5790 RETURN
5800 !
5810 ! SUBROUTINE TO READ AND DISPLAY A THRESHOLD SETTING
5820 M$="NO DATA READ"
5830 ENTER A ; M$
5840 WAIT 1000
5850 CLEAR
5860 DISP "The correct value for this      threshold should be :
5870 DISP L$
5880 DISP
5890 DISP "The returned value for this     threshold is :
5900 DISP M$
5910 IF L$=M$ THEN R=R*1
5920 IF L$<>M$ THEN R=R*0
5930 DISP
5940 DISP F$
```

Table 4-1. HP-IB Operation Verification Program Listing (Continued)

```
5950 PAUSE
5960 RETURN
5970 !
5980 ! SUBROUTINE TO INFORM USER THAT THE HP 85 HAS VERIFIED THE TEST
5990 CLEAR
6000 IF R=1 THEN GOTO 6050
6010 R(S)=1
6020 DISP "The HP 85 has verified that the 5005B failed this checkpoint."
6030 WAIT 3000
6040 RETURN
6050 R(S)=2
6060 DISP "The HP 85 has verified that the 5005B passed this checkpoint."
6070 WAIT 3000
6080 RETURN
```

Table 4-2. Operation Verification Test Record

5005B S/N _____ Date _____

PARAGRAPH NO.	TEST	PASS/FAIL RESULTS
4-10	Self-Check	_____
4-11	Polarity Edge Select Verification	_____
4-12	Threshold Family Select	_____
4-13	Noise MRG Adjust Verification	_____
4-14	Data Probe Switch Verification	_____
4-15	Frequency Counter Test	_____
4-16	Totalizing Counter Test	_____
4-17	Time Interval Test	_____
4-18	Ohmmeter Test	_____
4-19	Voltmeter Test	_____
4-22	NORMAL Mode Test	_____
4-23	QUAL Mode Test	_____
4-24	HP-IB Test	(Attach copy of results on back) _____

Table 4-2. Operation Verification Test Record (Continued)

5005B S/N _____ Date _____

PARAGRAPH NO.	TEST	CHECKPOINT RESULTS
4-24	HP-IB Test	Attach results here

SECTION V
ADJUSTMENTS

5-1. INTRODUCTION

5-2. This section describes the adjustments which will return the 5005B to peak operating condition after repairs are completed. If the adjustments are to be considered valid, the 5005B line voltage must be within +5% to -10% of nominal.

5-3. In general, periodic adjustment should not be necessary. However, to assure proper calibration, it is recommended that these adjustments be performed whenever repairs are made or the instrument fails the Operation Verification procedures in Section IV. The adjustment procedures in *Table 5-1* are listed in numeric order according to the assembly number. The order of adjustment is not critical; the procedures are in numeric order only for quick and easy reference.

5-4. SAFETY CONSIDERATIONS

5-5. Although the 5005B has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which MUST be followed to ensure safe operation and to retain the 5005B in safe condition (also see Section VIII of this manual). Service and adjustments should be performed only by qualified personnel.

WARNING

ANY INTERRUPTION OF THE PROTECTIVE (GROUNDING) CONDUCTOR OR DISCONNECTION OF THE PROTECTIVE EARTH TERMINAL IS LIKELY TO MAKE THE 5005B DANGEROUS.

WARNING

THE A2 DVM PRINTED CIRCUIT BOARD IS A HIGH IMPEDANCE PC BOARD. IT IS EXTREMELY SENSITIVE TO CONTAMINATION FROM DIRT AND OILS, APPLIED WHEN HANDLING WITH BARE HANDS. CONTAMINATION CAN CAUSE NONLINEARITY, DRIFT, OR INOPERATION. DO NOT HANDLE THE A2 DVM ASSEMBLY WITH BARE FINGERS, EXCEPT AT THE EDGES. REFER TO PARAGRAPH 8-56 FOR PROPER HANDLING AND CLEANING PROCEDURES.

5-6. Any adjustment, maintenance, or repair of the opened 5005B with voltage applied should be avoided as much as possible, and when inevitable, should be carried out by a skilled person who is aware of the hazard involved. Capacitors inside the 5005B may still be charged even if the 5005B has been disconnected from its source of supply.

5-7. Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of repaired fuses and the short circuiting of fuseholders must be avoided. Whenever it is likely that the protection offered by fuses has been impaired, the 5005B must be rendered inoperative and secured against any operation until repaired.

WARNING

ADJUSTMENTS DESCRIBED HEREIN ARE PERFORMED WITH POWER SUPPLIED TO THE 5005B WHILE THE PROTECTIVE COVERS ARE REMOVED. ENERGY AVAILABLE AT THE REAR PANEL LINE MODULE MAY, IF CONTACTED, RESULT IN PERSONAL INJURY.

5-8. EQUIPMENT REQUIRED

5-9. The test equipment required for the adjustments is listed in *Table 1-2, Recommended Test Equipment*. The critical specifications of any substitute test equipment must meet or exceed the standards listed in *Table 1-2* if the 5005B is to meet the specifications in *Table 1-1*.

5-10. ADJUSTMENT LOCATIONS

5-11. As an adjustment aid, *Figures 5-1* and *5-8* are provided to quickly locate and identify adjustment points in the instrument. These photos show variable resistors, variable capacitors, test points, etc., needed for adjustment of the instrument.

Table 5-1. Adjustments

Procedure	Assembly	Adjustment	Comments
Input Compensation Adjustments	A1	C7	Data Probe Input
	A1	C8	Start/ST-SP Input
	A1	C9	Stop/Qual Input
	A1	C10	Clock Input
Precision Reference Voltage Adjustment	A2	R2	Set for +10.000 Vdc

5-12. ADJUSTMENT PROCEDURES

5-13. Input Compensation Adjustments

5-14. The following procedures are provided to fine tune the high frequency compensation circuits for the Data Probe and Pod inputs. The input circuitry is adjusted for minimum waveform distortion into each respective input comparator. This is accomplished by applying a square wave to each input and monitoring the corresponding comparator output. The comparator output is observed using an oscilloscope, while varying the dc offset of the input signal. If the input circuitry is adjusted to under-compensate, the rising edge of the waveform into the comparator will be slower, and any change in the dc offset of the input will affect the timing at the leading edge of the comparator output pulse. If the input circuitry is adjusted to over-compensate, the waveform at the comparator input will have an overshoot. At some dc offset value, the output pulse of the comparator will occur only for the duration of the overshoot, with the trailing edge timing dependent on the dc offset. In a properly compensated circuit, the dc offset of the input signal can cause the appearance or disappearance of the pulse at the comparator output, but will not affect its width.

5-15. The input compensation adjustment is made to produce minimum distortion in the leading and trailing edges of extremely fast input signals. It is important to use an input pulse generator with very fast transition times, typically 2 ns or better.

5-16. The following procedures will adjust each of the four inputs to the 5005B (Data Probe, ST-SP/START, QUAL/STOP, and CLOCK) such that each respective comparator output pulse appears and disappears cleanly, with no change in pulse width, as the input signal dc offset is varied.

5-17. Preliminary Adjustment Procedure

5-18. To perform the input compensation adjustments, access and locate the adjustments on the A1 Main Assembly by referring to *Figure 5-1*. Assemble and preset the test equipment as follows:

a. Refer to the disassembly procedures in Section VIII and remove the 5005B top cover, top strut, and bottom cover. Holding it in a horizontal position, rotate the instrument 90° (clockwise) for access to the adjustment points.

WARNING

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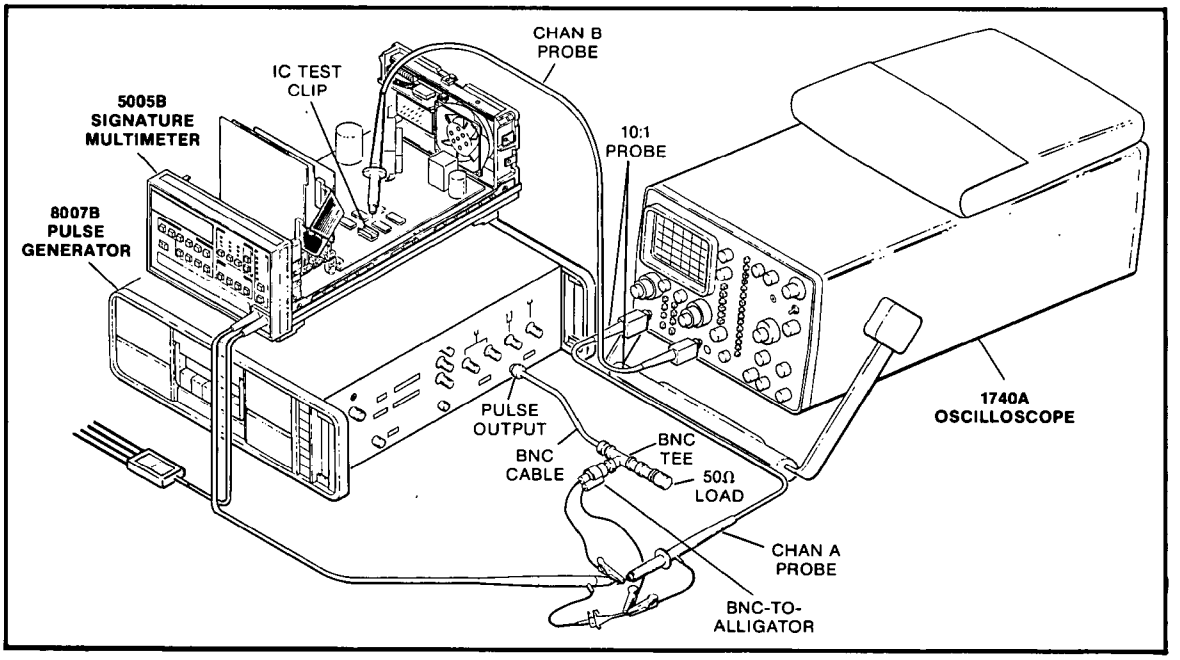
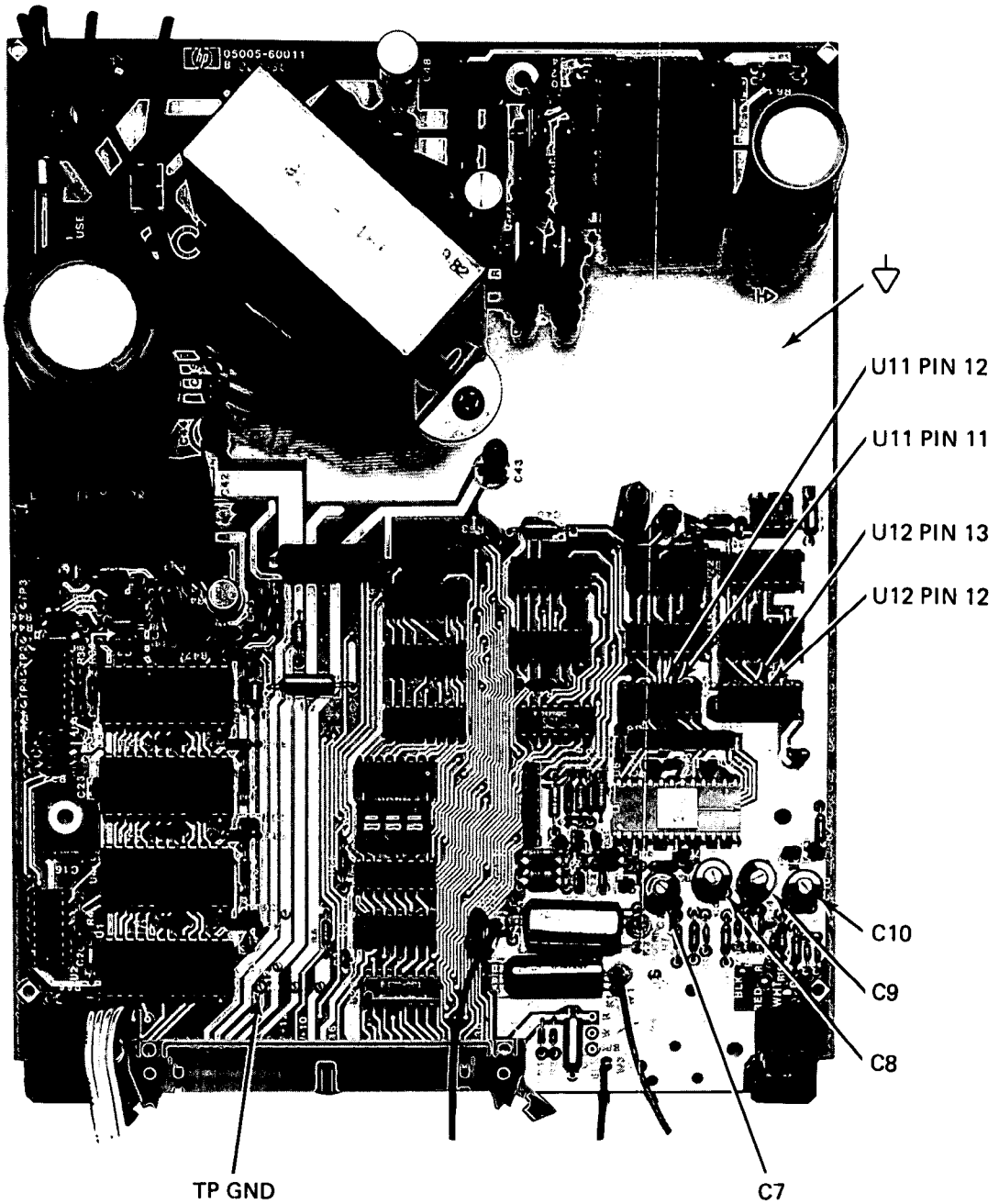
b. The top three printed circuit assemblies, A8 HP-IB Assembly, A2 DVM Assembly, and A3 Microprocessor Assembly are hinged for ease of service. Referring to the disassembly procedures in Section VIII, raise the A8 HP-IB, A2 DVM, and A3 Microprocessor assemblies on their hinges, allowing access to the adjustments and test points on A1 Main Assembly.

c. Set up the equipment as follows:





A1 MAIN ASSEMBLY

Figure 5-1. Input Compensation Adjustments

d. Set the HP1740A controls as follows:

CHANNEL A	DC coupled,.02 Volts/Div
CHANNEL B	DC coupled,.02 Volts/Div
SWEEP	AUTO
VERTICAL DISPLAY	ALT
HORIZONTAL DISPLAY	MAIN
INT TRIGGER	A
TIME/DIV	.2 ms

e. Set the pulse generator to output a square wave, ~500 mV p-p, at a 1 kHz rate. Adjust the leading and trailing edge controls for the fastest possible transition times, i.e., an "ideal" square wave. Set the pulse generator output dc offset to the adjustable mode. See *Figure 5-2*. If an HP 8007B is available, set the controls as follows:

RATE	.3K–10K
RATE VERNIER	Adjust for 1 kHz
PULSE DELAY	5 ns–50 ns (DELAY)
PULSE DELAY VERNIER	Fully CCW
PULSE WIDTH	50 μs–1.5 ms
PULSE WIDTH VERNIER	Adjust for 50-50 Duty Cycle
TRIGGER MODE	NORM
TRANSITION TIME	2.0 ns–0.1 μs
LEADING EDGE	Fully CCW
TRAILING EDGE	Fully CCW
AMPLITUDE	0.5–1.0V
AMPLITUDE VERNIER	Adjust for ~500 mV/p-p
OFFSET	ON
OFFSET VERNIER	Per Adjustment

f. Set the HP 5005B controls as follows:

LINE	ON
SIGNATURE	NORM
THRESHOLDS	TTL

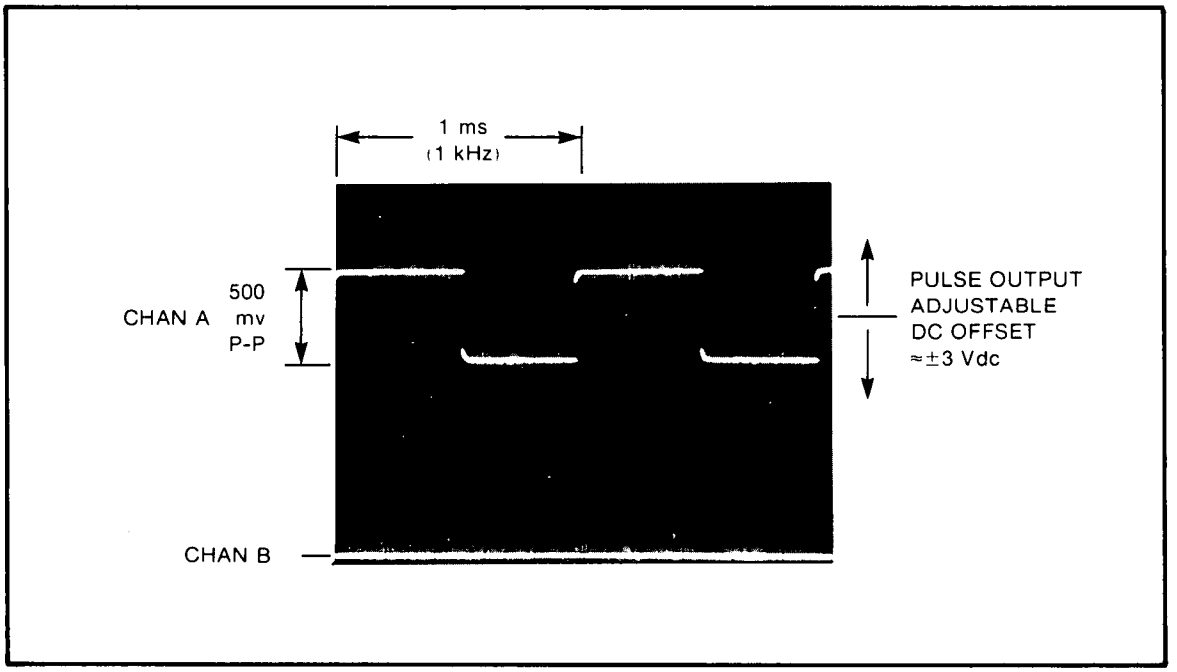


Figure 5-2. Pulse Generator Output

5-19. Input Compensation Adjustment Procedures (A1 Motherboard Assembly)

Input	Adjust	Connect Point
Data Probe	C7	A1 U12, pin 12
ST-SP/Start	C8	A1 U11, pin 12
Stop/Qual	C9	A1 U11, pin 13
Clock	C10	A1 U12, pin 13

a. Connect the Channel A oscilloscope probe to the pulse generator PULSE OUTPUT as shown in the set-up diagram.

b. Connect the Channel B oscilloscope probe to A1 U12, pin 12, and connect the ground clip to the 5005B rear panel.

c. Connect the 5005B Data Probe tip to the pulse generator PULSE OUTPUT. Connect the Data Probe ground wire to the closest ground connection.

d. Begin with the Pulse Generator OFFSET VERNIER set to the fully positive offset position. Using the OFFSET VERNIER, slowly lower the dc offset of the input signal until the comparator output on the oscilloscope Channel B "just" begins to trigger. This is indicated by a likeness of the input square wave on the oscilloscope Channel A, appearing on Channel B. The Channel A POSN control should be readjusted as necessary, to return the input waveform to the oscilloscope display. Readjust the OFFSET VERNIER slightly positive until the comparator output, on Channel B, intermittently triggers, displaying trailing edge jitter as shown in *Figure 5-3*.

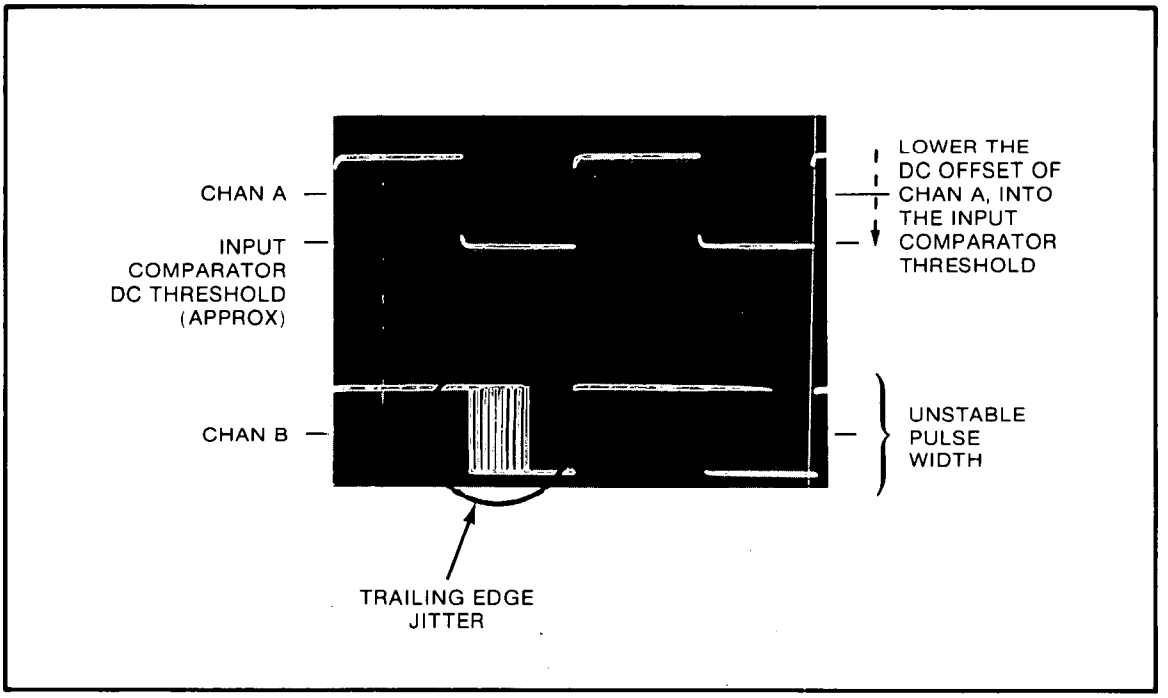


Figure 5-3. Under-Compensated

e. Using a nonmetallic screwdriver, adjust A1C7 for a stable, symmetrical square wave. Readjust the OFFSET VERNIER slightly positive again, until the trailing edge jitter reappears. Readjust A1C7. Repeat this routine until the capacitor (C7) is adjusted such that the comparator output on Channel B "snaps-in", displaying a stable symmetrical square wave as early as possible, while varying the input OFFSET VERNIER. When properly adjusted, the Channel B display may be intermittent, but the pulse width should not vary. That is, the comparator may be triggering at times, and not triggering at other times, producing an unstable display (see *Figure 5-4*), but there should be no trailing edge jitter and the pulse width should never be less than the 50-50 duty cycle shown in *Figure 5-5*.

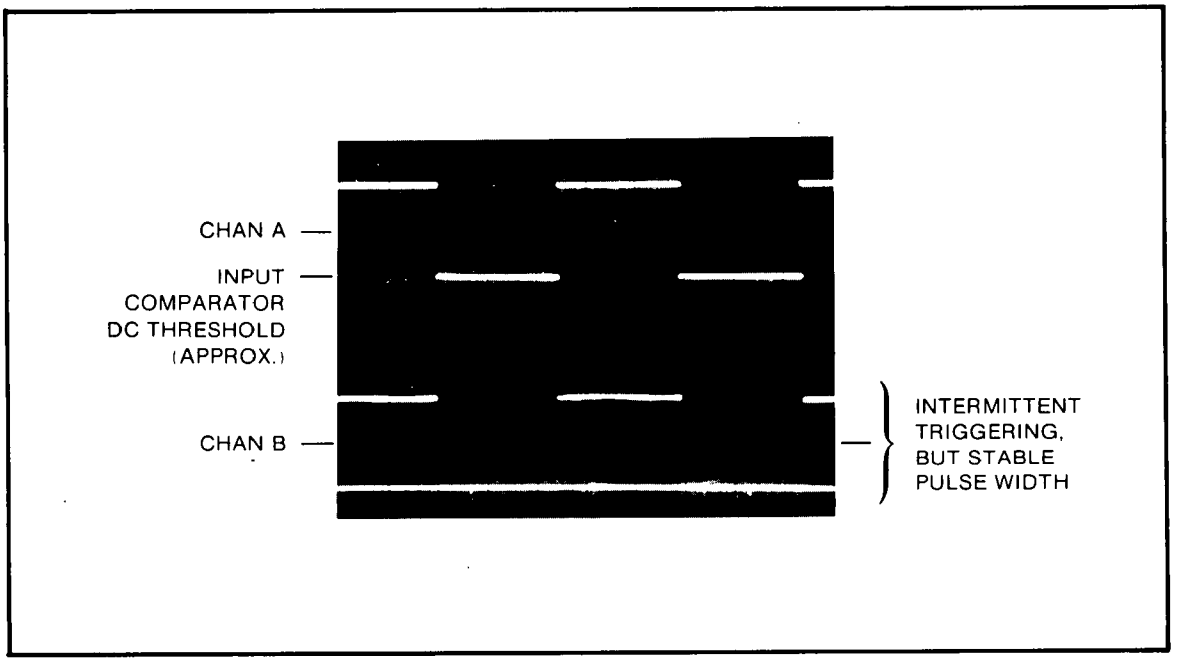


Figure 5-4. Proper Compensation (Intermittent)

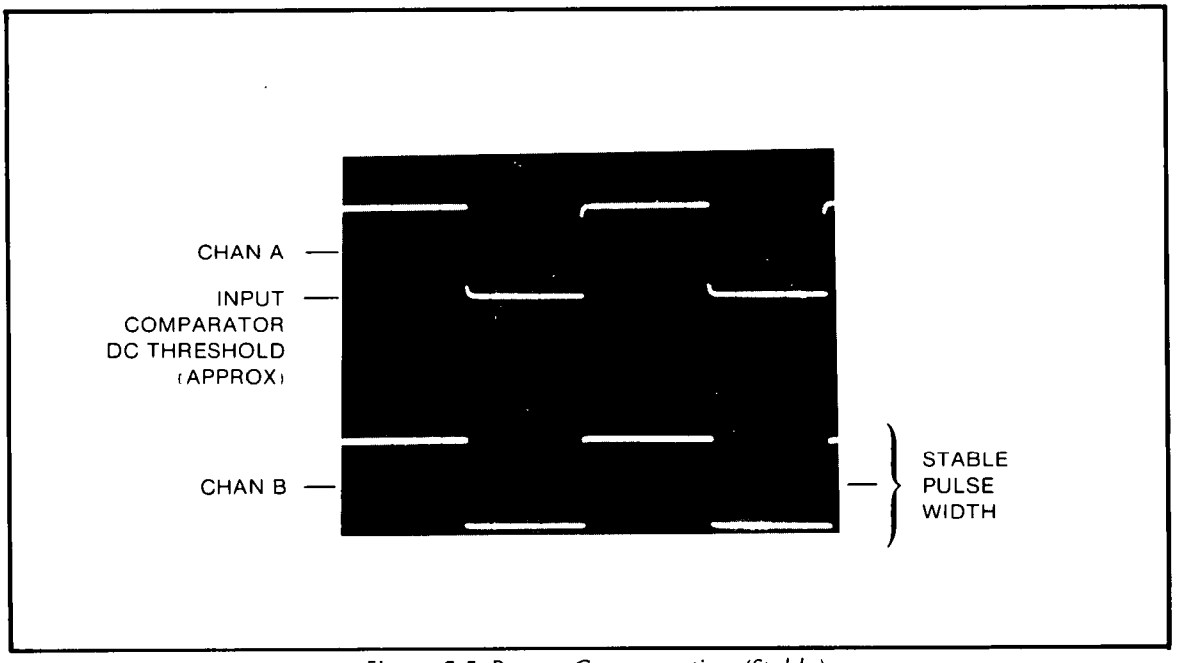


Figure 5-5. Proper Compensation (Stable)

f. Repeat the procedures in steps d. and e., with the OFFSET VERNIER set to the fully negative position. Ensure that the comparator output snaps in cleanly, with no leading edge jitter, as the dc offset of the input signal is raised into the comparator threshold. Refer to *Figures 5-6* and *5-7*.

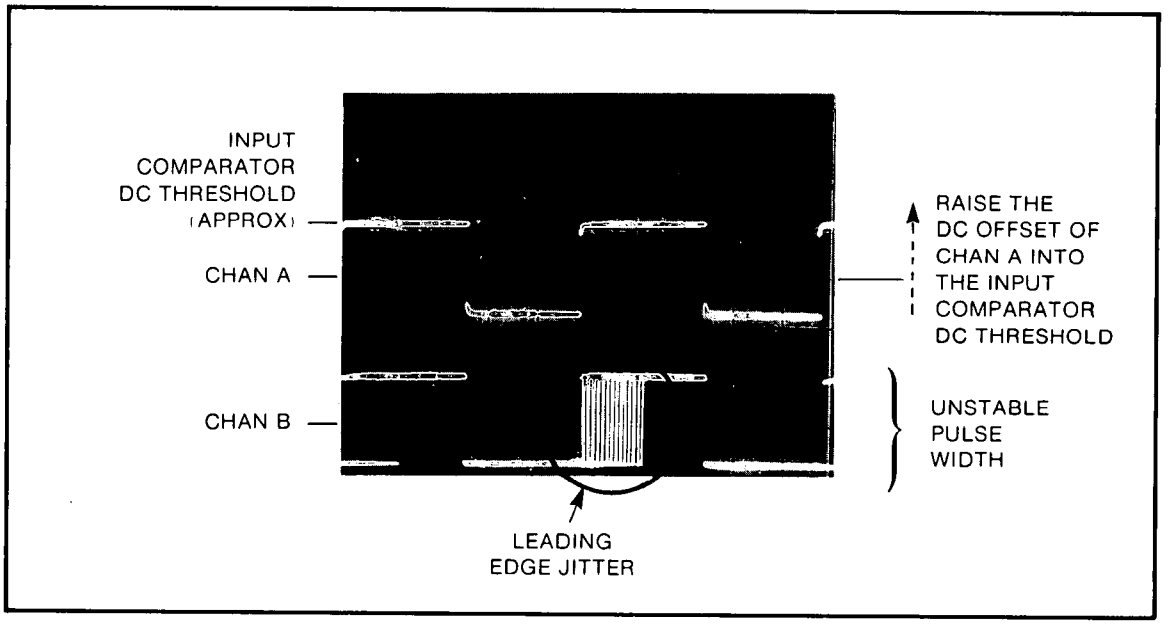


Figure 5-6. Over-Compensated

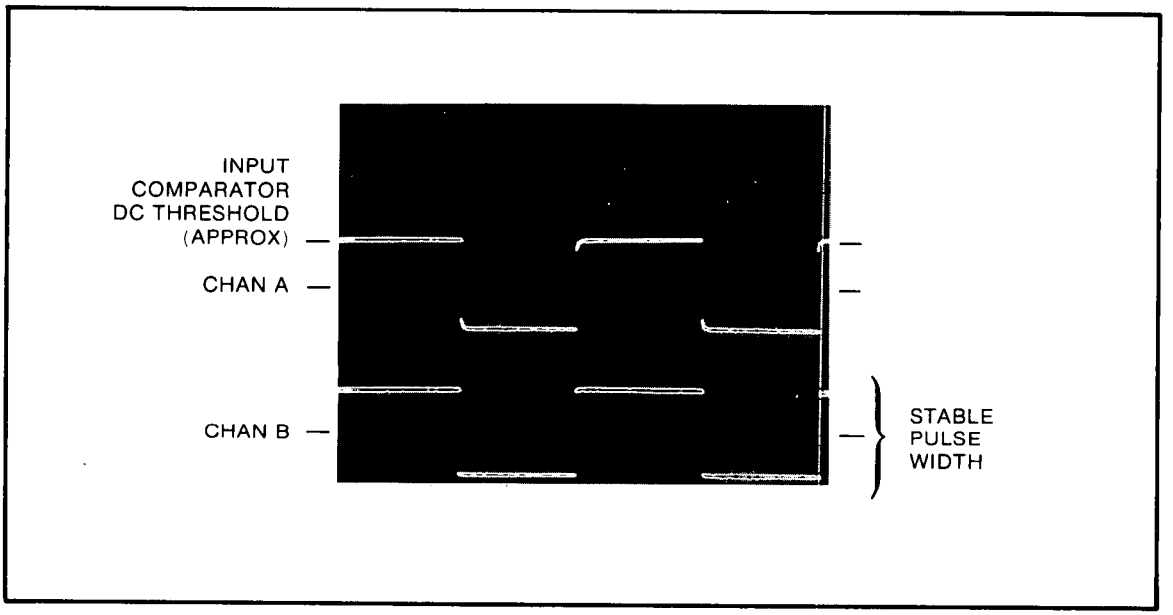


Figure 5-7. Proper Compensation

g. Disconnect the Data Probe and the Channel B oscilloscope probe.

h. Connect the Channel B oscilloscope probe to A1U11 pin 12, and connect the ground clip to the 5005B rear panel.

i. Connect the 5005B Pod START/ST-SP connector to the pulse generator PULSE OUTPUT. Connect the Pod ground (⊥) connector to the closest ground connection.

j. Repeat the procedures in steps d. through f., substituting C8 for C7.

k. Disconnect the 5005B Pod START/ST-SP connector.

l. Connect the Channel B oscilloscope probe to A1U11 pin 13, and connect the ground clip to the 5005B rear panel.

m. Connect the 5005B Pod STOP/QUAL connector to the pulse generator PULSE OUTPUT. Connect the Pod ground (⊥) connector to the closest ground connection.

n. Repeat the procedures in steps d. through f., substituting C9 for C7.

o. Disconnect the 5005B Pod STOP/QUAL connector.

p. Connect the Channel B oscilloscope probe to A1U12 pin 13, and connect the ground clip to the 5005B rear panel.

q. Connect the 5005B Pod CLOCK connector to the pulse generator PULSE OUTPUT. Connect the Pod ground (⊥) connector to the closest ground connection.

r. Repeat the procedures in steps d. through f., substituting C10 for C7.

s. This completes the input compensation adjustments.

5-20. Precision Reference Voltage Adjustment (A2 DVM Assembly)

5-21. The following procedure adjusts and verifies the +10.00 Vdc precision reference voltage, on the A2 DVM Assembly. The only test equipment required is a Digital Voltmeter. Refer to *Table1-2*, for the minimum specification requirements for test equipment.

WARNING

THE A2 DVM PRINTED CIRCUIT BOARD IS A HIGH IMPEDANCE PC BOARD. IT IS EXTREMELY SENSITIVE TO CONTAMINATION FROM DIRT AND OILS, APPLIED WHEN HANDLING WITH BARE HANDS. CONTAMINATION CAN CAUSE NONLINEARITY, DRIFT, OR INOPERATION. DO NOT HANDLE THE A2 DVM ASSEMBLY WITH BARE FINGERS, EXCEPT AT THE EDGES. REFER TO PARAGRAPH 8-56 FOR PROPER HANDLING AND CLEANING PROCEDURES.

5-22. To perform the +10.00V Precision Reference adjustment, refer to *Figure 5-8*, and access the adjustment and test points on the A2 DVM Assembly. Assemble and preset the test equipment as follows:

a. Refer to the disassembly procedures in Section VIII and remove the 5005B top cover, top strut, and bottom cover. Holding it in a horizontal position, rotate the instrument 90° (clockwise) for access to the adjustment points.

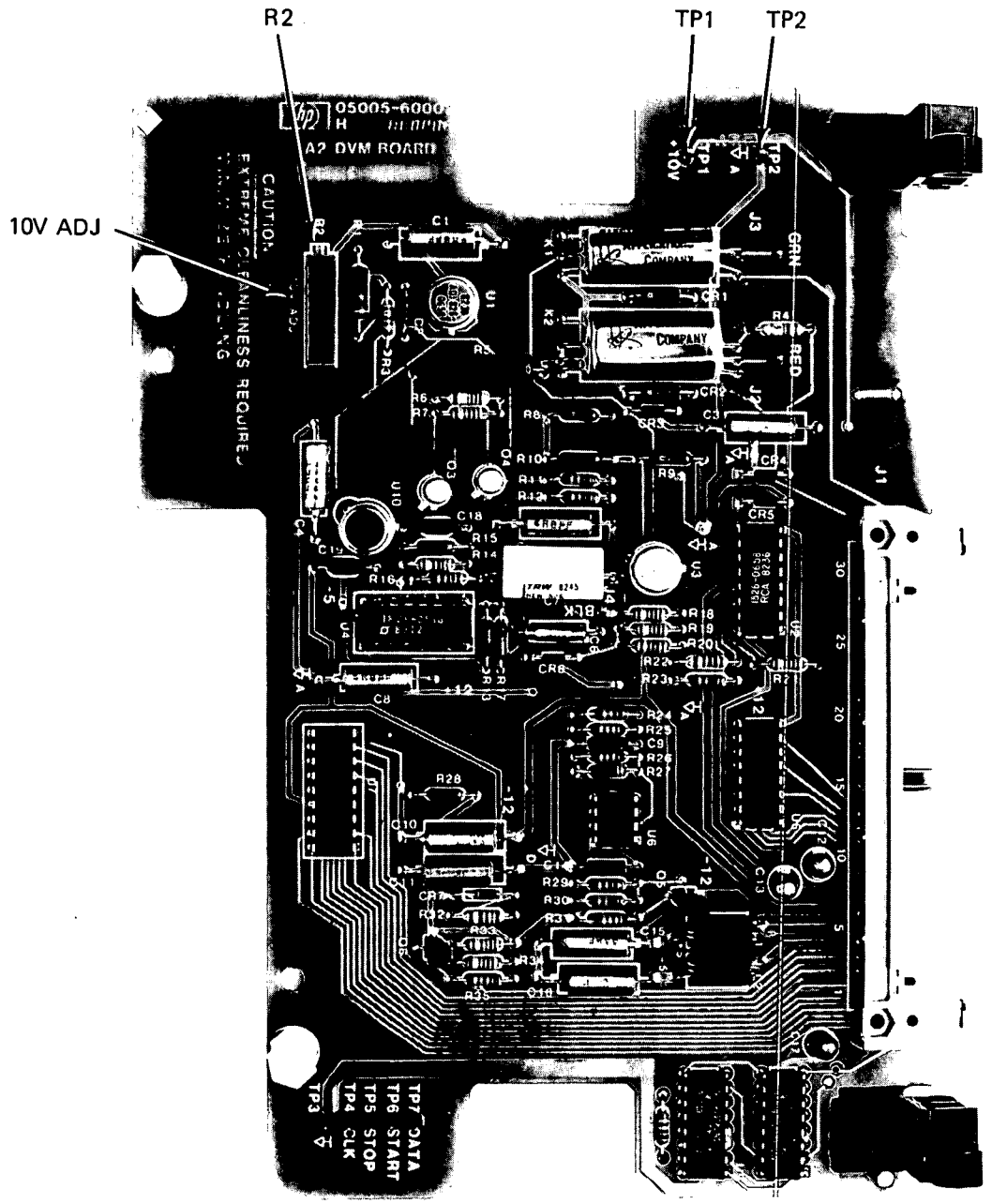
b. The top three printed circuit assemblies, A8 HP-IB Assembly, A3 Microprocessor Assembly, and A2 DVM Assembly are hinged for ease of serviceability. Referring to the disassembly procedures in Section VIII, raise the A8 and A3 assemblies on their hinges to allow access to the adjustment and test points on the A2 DVM Assembly.

c. Connect the DVM positive lead to A2 DVM Assembly TP1 (+10V), and negative lead to A2TP2 (ground).

d. Set 5005B LINE switch to ON.

e. Adjust A2R2 for a reading of +10.000 ±.001V.

f. Disconnect all test equipment. This completes the adjustment of the Precision Reference Voltage.



A2 DVM ASSEMBLY

Figure 5-8. +10.00V Precision Reference Adjustment

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering parts. *Table 6-1* lists abbreviations used in the parts list and throughout the manual. *Table 6-2* lists all replaceable parts in reference designation order. *Table 6-3* contains the names and addresses that correspond to the manufacturer's code numbers.

6-3. ABBREVIATIONS

6-4. *Table 6-1* lists abbreviations used in the parts list, and throughout the manual. In some cases, two forms of the abbreviations are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lower and upper case letters.

6.5. REPLACEABLE PARTS LIST

6-6. *Table 6-2* is the list of replaceable parts and is organized as follows:

a. Electrical assemblies and their components in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

c. Miscellaneous parts.

6-7. The information given for each part consists of the following:

a. The Hewlett-Packard part number.

b. Part number check digit (CD).

c. The total quantity (Qty) in the assembly.

d. The description of the part.

e. A typical manufacturer of the part in a five-digit code.

f. The manufacturer's number of the part.

6-8. The total quantity for each part is given only once — at the first appearance of the part number in the list.

6-9. MANUFACTURER'S CODE LIST

6-10. *Table 6-3* contains the names and addresses that correspond to the manufacturer's code numbers.

6-11. ORDERING INFORMATION

6-12. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, the check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

6-13. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Office.

6-14. DIRECT MAIL ORDER SYSTEM

6-15. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices — to provide these advantages, a check or money order must accompany each order.

6-16. Mail order forms and specific ordering information is available through your HP office. Addresses and phone numbers are located at the back of this manual.

6-17. CABINET PARTS AND HARDWARE

6-18. To locate and identify miscellaneous cabinet parts and instrument hardware, refer to *Figures 6-1* through *6-6*. These figures provide various exploded views of the instrument, identified with Reference Designators. A table is provided opposite each illustration, containing part number, description, and quantity information for each reference designator shown. The quantity indicated represents the total number used in the subassembly.

Table 6-1. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	DL	= delay line	K	= relay	T	= transformer
AT	= attenuator; isolator; termination	DS	= annunciator; signaling device (audible or visual); lamp; LED	L	= coil; inductor	TB	= terminal board
B	= fan; motor	E	= miscellaneous electrical part	M	= metre	TC	= thermocouple
BT	= battery	F	= fuse	MP	= miscellaneous mechanical part	TP	= test point
C	= capacitor	FL	= filter	P	= electrical connector (movable portion); plug	U	= integrated circuit; microcircuit
CP	= coupler	H	= hardware	Q	= transistor; SCR; triode thyristor	V	= electron tube
CR	= diode; diode thyristor; varactor	HY	= circulator	R	= resistor	VR	= voltage regulator; breakdown diode
DC	= directional coupler	J	= electrical connector (stationary portion); jack	RT	= thermistor	W	= cable; transmission path; wire
				S	= switch	X	= socket
						Y	= crystal unit-piezo-electric
						Z	= tuned cavity; tuned circuit

ABBREVIATIONS

A	= ampere	HD	= head	NE	= neon	SPST	= single-pole, single-throw
ac	= alternating current	HDW	= hardware	NEG	= negative	SSB	= single sideband
ACCESS	= accessory	HF	= high frequency	nF	= nanofarad	SST	= stainless steel
ADJ	= adjustment	HG	= mercury	NI PL	= nickel plate	STL	= steel
A/D	= analog-to-digital	HI	= high	N/O	= normally open	SQ	= square
AF	= audio frequency	HP	= Hewlett-Packard	NOM	= nominal	SWR	= standing-wave ratio
AFC	= automatic frequency control	HPF	= high pass filter	NORM	= normal	SYNC	= synchronize
AGC	= automatic gain control	HR	= hour (used in parts list)	NPN	= negative-positive-negative	T	= timed (slow-blow fuse)
AL	= aluminum	HV	= high voltage	NPO	= negative-positive zero (zero temperature coefficient)	TA	= tantalum
ALC	= automatic level control	Hz	= hertz	NRFR	= not recommended for field replacement	TC	= temperature compensating
AM	= amplitude modulation	IC	= integrated circuit	ns	= nanosecond	TD	= time delay
AMPL	= amplifier	ID	= inside diameter	NSR	= not separately replaceable	TERM	= terminal
APC	= automatic phase control	IF	= intermediate frequency	nW	= nanowatt	TFT	= thin-film transistor
ASSY	= assembly	IMPG	= impregnated	OBD	= order by description	TGL	= toggle
AUX	= auxiliary	in	= inch	OD	= outside diameter	THD	= thread
AVG	= average	INCD	= incandescent	OH	= oval head	THRU	= through
AWG	= american wire gauge	INCL	= include(s)	OP AMP	= operational amplifier	TI	= titanium
BAL	= balance	INP	= input	OPT	= option	TOL	= tolerance
BCD	= binary coded decimal	INS	= insulation	OSC	= oscillator	TRIM	= trimmer
BD	= board	INT	= internal	OX	= oxide	TSTR	= transistor
BE CU	= beryllium copper	kg	= kilogram	oz	= ounce	TTL	= transistor-transistor logic
BFO	= beat frequency oscillator	kHz	= kilohertz	Ω	= ohm	TV	= television
BH	= binder head	kΩ	= kilohm	P	= peak (used in parts list)	TVI	= television interference
BKDN	= breakdown	kV	= kilovolt	PAM	= pulse-amplitude modulation	TWT	= traveling wave tube
BP	= bandpass	lb	= pound	PC	= printed circuit	U	= micro (10^{-6}) used in parts list)
BPF	= bandpass filter	LC	= inductance-capacitance	PCM	= pulse-code modulation; pulse-count modulation	UF	= microfarad (used in parts list)
BRS	= brass	LED	= light-emitting diode	PDM	= pulse-duration modulation	UHF	= ultrahigh frequency
BWO	= backward-wave oscillator	LF	= low frequency	pF	= picofarad	UNREG	= unregulated
CAL	= calibrate	LG	= long	PH BRZ	= phosphor bronze	V	= volt
ccw	= counterclockwise	LH	= left hand	PHL	= phillips	VA	= voltampere
CER	= ceramic	LIM	= limit	PIN	= positive-intrinsic-negative	Vac	= volts ac
CHAN	= channel	LIN	= linear taper (used in parts list)	PIV	= peak inverse voltage	VAR	= variable
cm	= centimeter	lin	= linear	pk	= peak	VCO	= voltage-controlled oscillator
CMO	= coaxial	LK WASH	= lockwasher	PL	= phase lock	Vdc	= volts dc
COEF	= coefficient	LO	= low; local oscillator	PLO	= phase lock oscillator	VDCW	= volts, dc, working (used in parts list)
COM	= common	LOG	= logarithmic taper (used in parts list)	PM	= phase modulation	V(F)	= volts, filtered
COMP	= composition	log	= logarithm(ic)	PNP	= positive-negative-positive	VFO	= variable-frequency oscillator
COMPL	= complete	LPF	= low pass filter	P/O	= part of	VHF	= very-high frequency
CONN	= connector	LV	= low voltage	POLY	= polystyrene	Vpk	= volts peak
CP	= cadmium plate	m	= metre (distance)	PORC	= porcelain	Vp-p	= volts peak-to-peak
CRT	= cathode-ray tube	mA	= milliampere	POS	= positive; position(s) (used in parts list)	Vrms	= volts rms
CTL	= complementary transistor logic	MAX	= maximum	POSN	= position	VSWR	= voltage standing wave ratio
CW	= continuous wave	MΩ	= megohm	POT	= potentiometer	VTO	= voltage-tuned oscillator
cw	= clockwise	MEG	= meg (10^6) (used in parts list)	p-p	= peak-to-peak	VTVM	= vacuum-tube voltmeter
D/A	= digital-to-analog	MET FLM	= metal film	PP	= peak-to-peak (used in parts list)	V(X)	= volts, switched
dB	= decibel	MET OX	= metal oxide	PPM	= pulse-position modulation	W	= watt
dBm	= decibel referred to 1 mW	MF	= medium frequency; microfarad (used in parts list)	PREAMPL	= preamplifier	W/	= with
dc	= direct current	MFR	= manufacturer	PRF	= pulse-repetition frequency	WIV	= working inverse voltage
deg	= degree (temperature interval or difference)	mg	= milligram	PRR	= pulse repetition rate	WW	= wirewound
... °	= degree (plane angle)	MHz	= megahertz	ps	= picosecond	W/O	= without
°C	= degree Celsius (centrigrade)	mH	= millihenry	PT	= point	YIG	= yttrium-iron-garnet
°F	= degree Fahrenheit	mho	= conductance	PTM	= pulse-time modulation	Zo	= characteristic impedance
°K	= degree Kelvin	MIN	= minimum	PWM	= pulse-width modulation		
DEPC	= deposited carbon	min	= minute (time)	PWV	= peak working voltage		
DET	= detector	... '	= minute (plane angle)	RC	= resistance capacitance		
diam	= diameter	MINAT	= miniature	RECT	= rectifier		
DIA	= diameter (used in parts list)	mm	= millimetre	REF	= reference		
DIFF AMPL	= differential amplifier	MOD	= modulator	REG	= regulated		
div	= division	MOM	= momentary	REPL	= replaceable		
DPDT	= double-pole, double-throw	MOS	= metal-oxide semiconductor	RF	= radio frequency		
DR	= drive	ms	= millisecond	RFI	= radio frequency interference		
DSB	= double sideband	MTG	= mounting	RH	= round head; right hand		
DTL	= diode transistor logic	MTR	= meter (indicating device)	RLC	= resistance-inductance-capacitance		
DVM	= digital voltmeter	mV	= millivolt	RMO	= rack mount only		
ECL	= emitter coupled logic	mVac	= millivolt, ac	rms	= root-mean-square		
EMF	= electromotive force	mVdc	= millivolt, dc	RND	= round		
EDP	= electronic data processing	mVpk	= millivolt, peak	ROM	= read-only memory		
ELECT	= electrolytic	mVp-p	= millivolt, peak-to-peak	R&P	= rack and panel		
ENCAP	= encapsulated	mVrms	= millivolt, rms	RWV	= reverse working voltage		
EXT	= external	mW	= milliwatt	S	= scattering parameter		
F	= farad	MUX	= multiplex	s	= second (time)		
FET	= field-effect transistor	MY	= mylar	... "	= second (plane angle)		
F/F	= flip-flop	μA	= microampere	S-B	= slow-blow fuse (used in parts list)		
FH	= flat head	μF	= microfarad	SCR	= silicon controlled rectifier; screw		
FOL H	= fillister head	μH	= microhenry	SE	= selenium		
FM	= frequency modulation	μmho	= micromho	SECT	= sections		
FP	= front panel	μs	= microsecond	SEMICON	= semiconductor		
FREQ	= frequency	μV	= microvolt	SHF	= superhigh frequency		
FXD	= fixed	μVac	= microvolt, ac	SI	= silicon		
g	= gram	μVdc	= microvolt, dc	SIL	= silver		
GE	= germanium	μVpk	= microvolt, peak	SL	= slide		
GHz	= gigahertz	μVp-p	= microvolt, peak-to-peak	SNR	= signal-to-noise ratio		
GL	= glass	μVrms	= microvolt, rms	SPDT	= single-pole, double-throw		
GND	= ground(ed)	μW	= microwatt	SPG	= spring		
H	= henry	nA	= nanoampere	SR	= split ring		
h	= hour	NC	= no connection				
HET	= heterodyne	N/C	= normally closed				
HEX	= hexagonal						

NOTE

All abbreviations in the parts list will be in upper case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

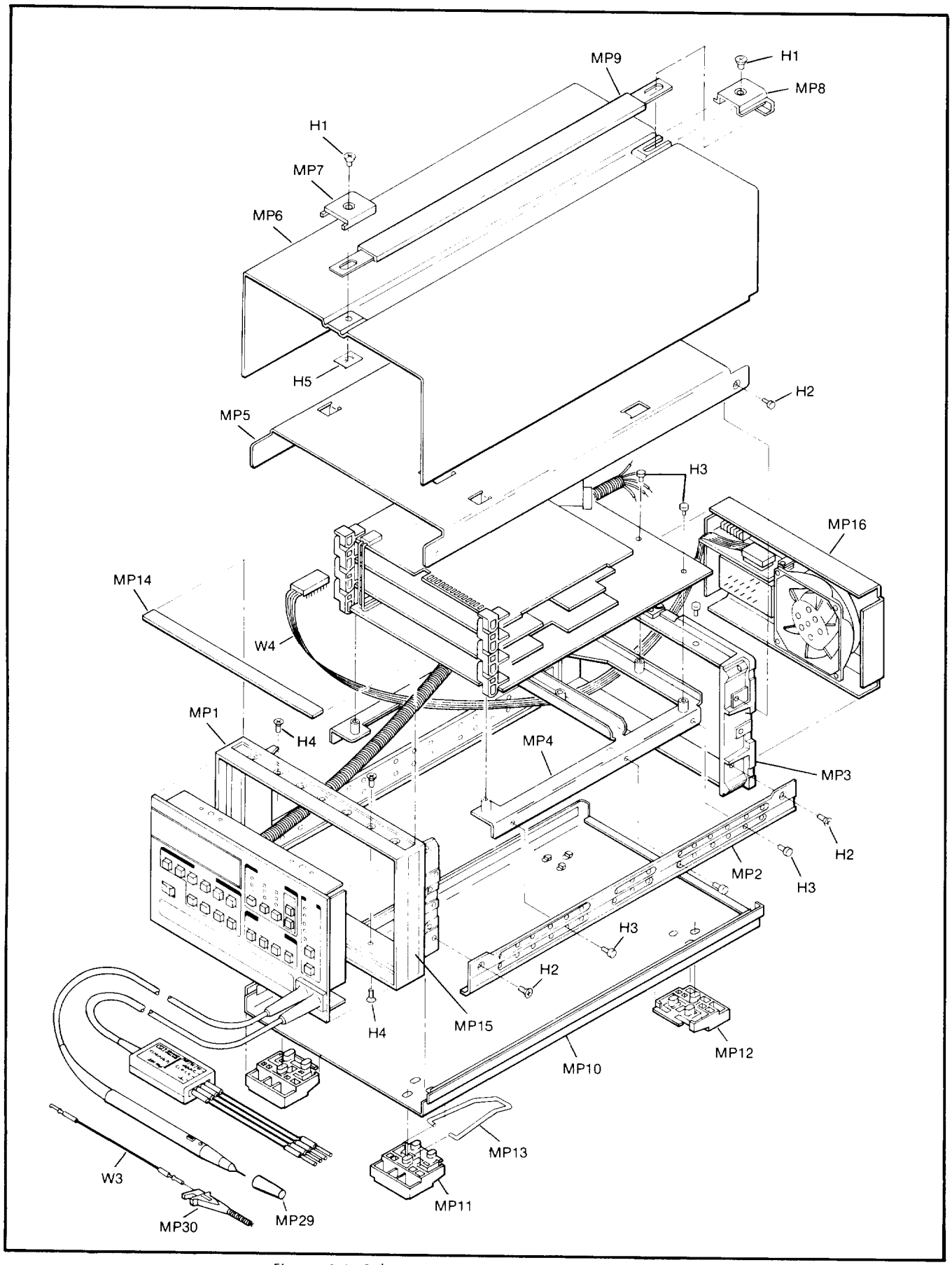


Figure 6-1. Cabinet Parts and Hardware (External)

REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
MP1	5020-8815	CASTING, FRONT FRAME	1
MP2	5020-8836	STRUT	2
MP3	5020-8816	CASTING, REAR FRAME	1
MP4	05005-00012	SUPPORT - PCB	1
MP5	05005-00011	STRUT - TOP	1
MP6	05005-00007	COVER - TOP	1
MP7	5040-7219	STRAP - HANDLE CAP FRONT	1
MP8	5040-7220	STRAP - HANDLE CAP REAR	1
MP9	5060-9803	STRAP HANDLE	1
MP10	5060-9964	COVER - BOTTOM	1
MP11	5040-7201	FOOT	2
MP12	5040-7222	FOOT - NONSKID	2
MP13	1460-1345	TILT STAND SST	2
MP14	5040-7203	TRIM, TOP 1/2	1
MP15	5001-0439	TRIM, FRONT SIDE	2
MP16	05005-00008	PANEL - REAR	1
MP29	00547-40005	COVER - PROBE TIP	1
MP30	10230-62101	GRABBER	5
H1	2680-0172	SCREW-MACH 10-32 .375LG 100 DEG	2
H2	2510-0192	SCREW-MACH 8-32 .25 LG 100 DEG	12
H3	0515-0212	SCREW MACH M3.5×0.6 6MM-LG PAN HEAD	14
H4	0515-0218	SCREW-MACH M3.5×0.6 6MM-LG	4
H5	0590-0639	NUT-SHEET METAL FLAT 10-32	1
W3	05005-60116	PROBE GROUND	1
W4	8120-3466	CABLE ASSEMBLY, 24-PIN FLAT	1

Part of Figure 6-1. Cabinet Parts and Hardware (External)

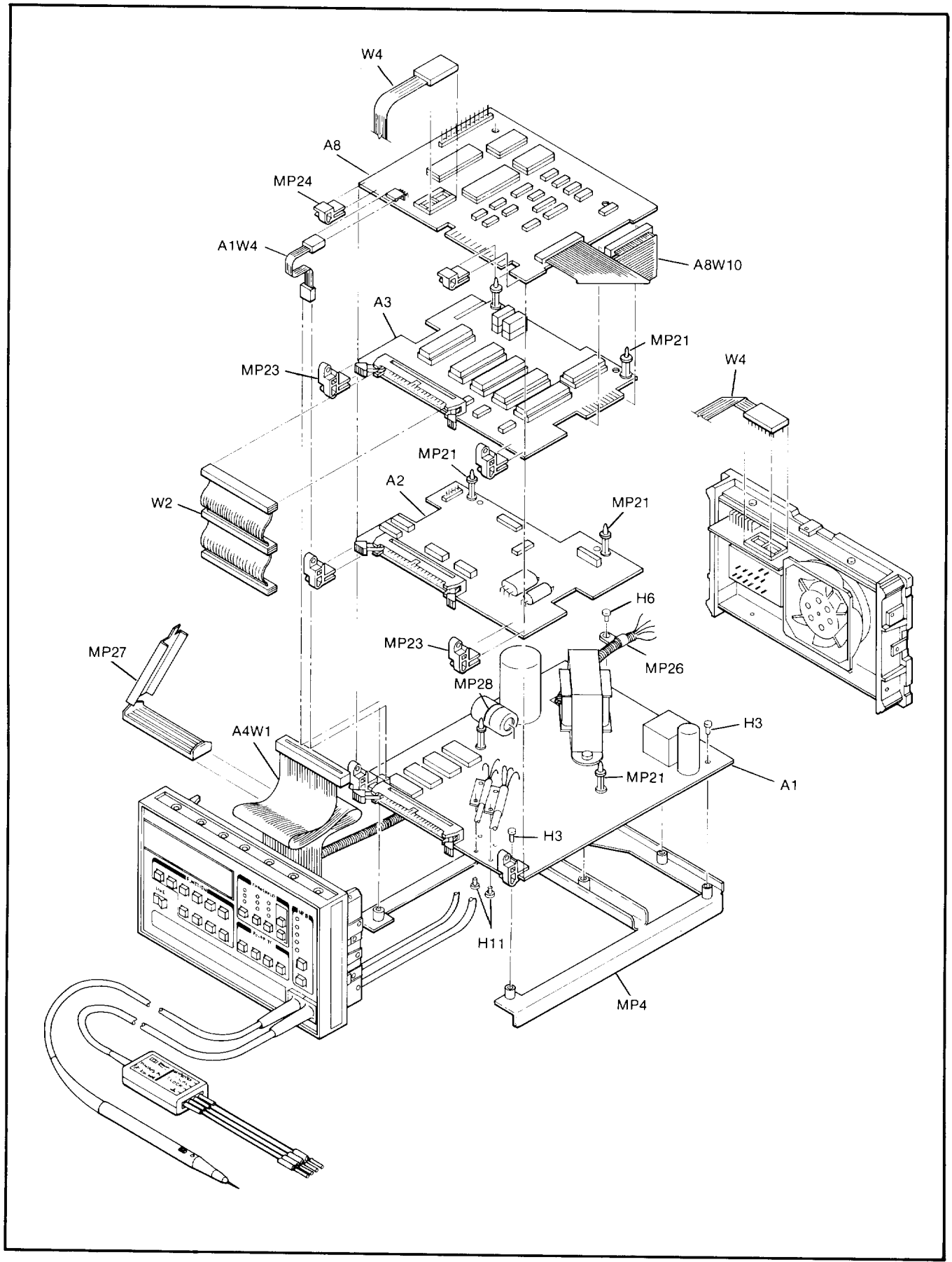
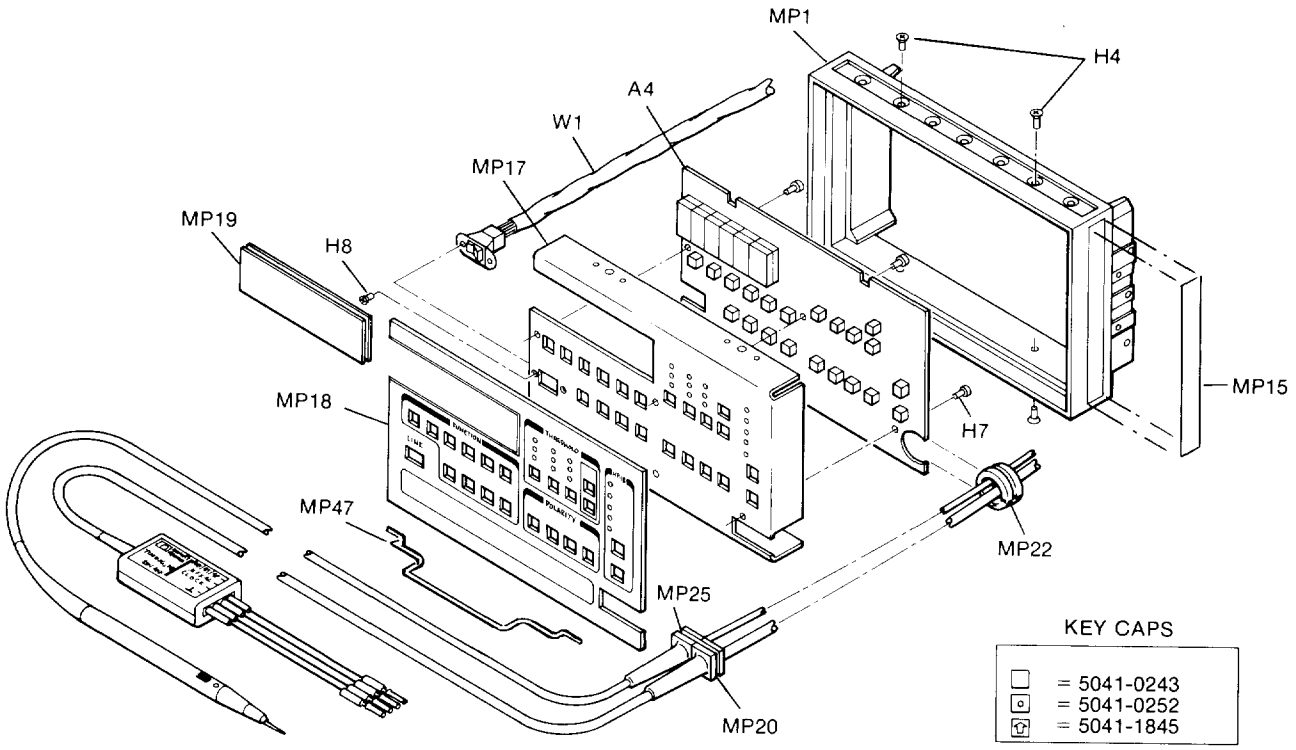


Figure 6-2. Cabinet Parts and Hardware (Internal)

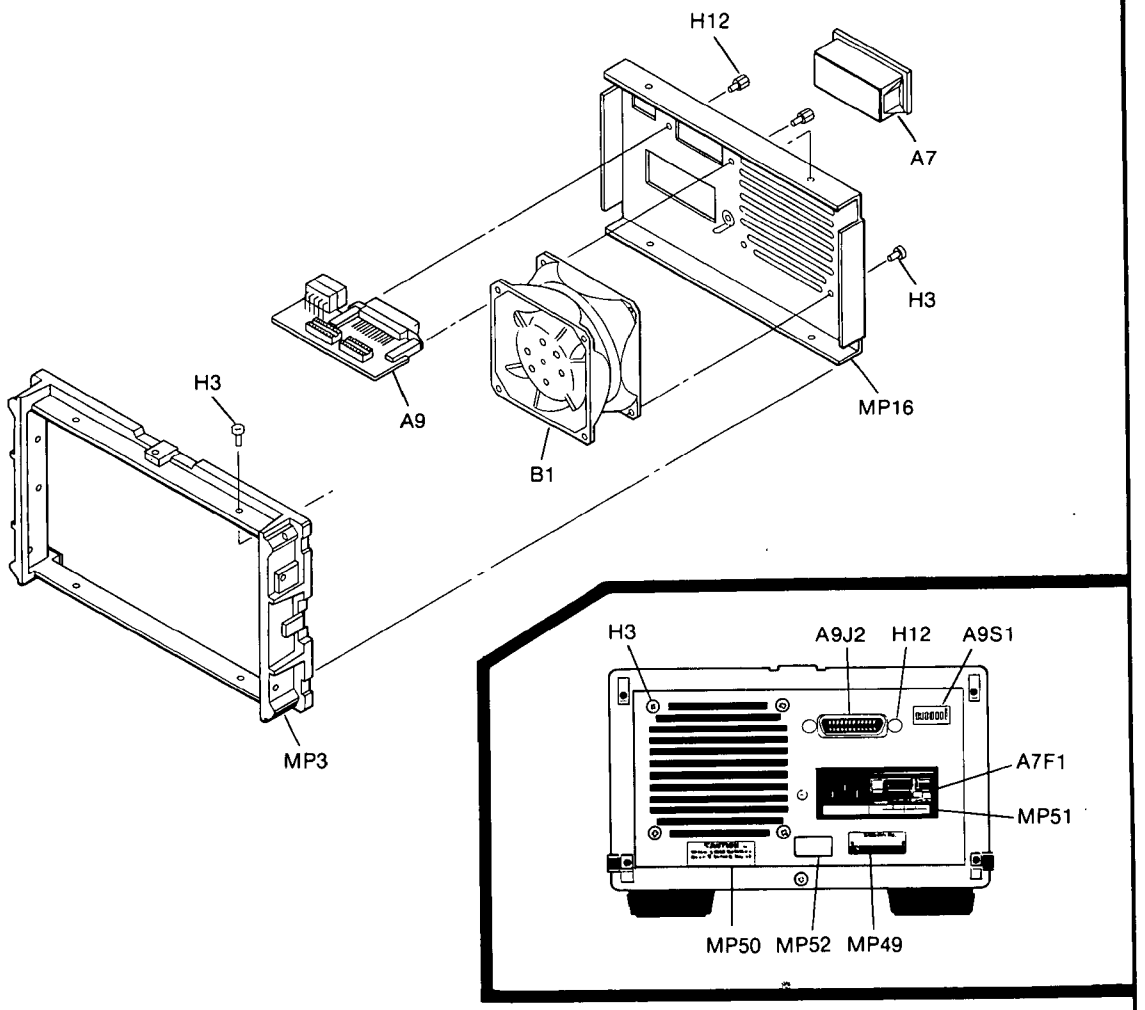
REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
MP4	05005-00012	SUPPORT-PCB	1
MP21	0380-0630	SPACER, SNAP-IN .75LG	6
MP23	5040-7721	HINGLE-FULL	6
MP24	5040-7787	HINGE-HALF	2
MP26	1400-0249	CABLE TIE	1
MP27	1400-1140	CLAMP-FL-CA NYL	1
MP28	1400-0493	CABLE TIE	1
H3	0515-0212	SCREW-MACH M3.5X0.6 6MM-LG	5
H6	0515-0413	SCREW-MACH M4X0.7 6MM-LG	4
H11	0624-0078	SCREW-TAPPING 6-32	6
A1	05005-60011	MAIN ASSEMBLY	1
A2	05005-60002	DVM ASSEMBLY	1
A3	05005-60012	MICROPROCESSOR ASSEMBLY	1
A8	05005-60007	HP-IB ASSEMBLY	1
A1W4	05005-60121	CABLE ASSEMBLY-DC JUMPER	1
A4W1	05005-60122	CABLE ASSEMBLY DISPLAY	1
A8W10	05005-60106	CABLE ASSEMBLY - 34 PIN	1
W2	05005-60104	CABLE ASSEMBLY, 60-PIN RIBBON	1
W4	8120-2466	CABLE ASSEMBLY 24-PIN FLAT	1

Part of Figure 6-2. Cabinet Parts and Hardware (Internal)



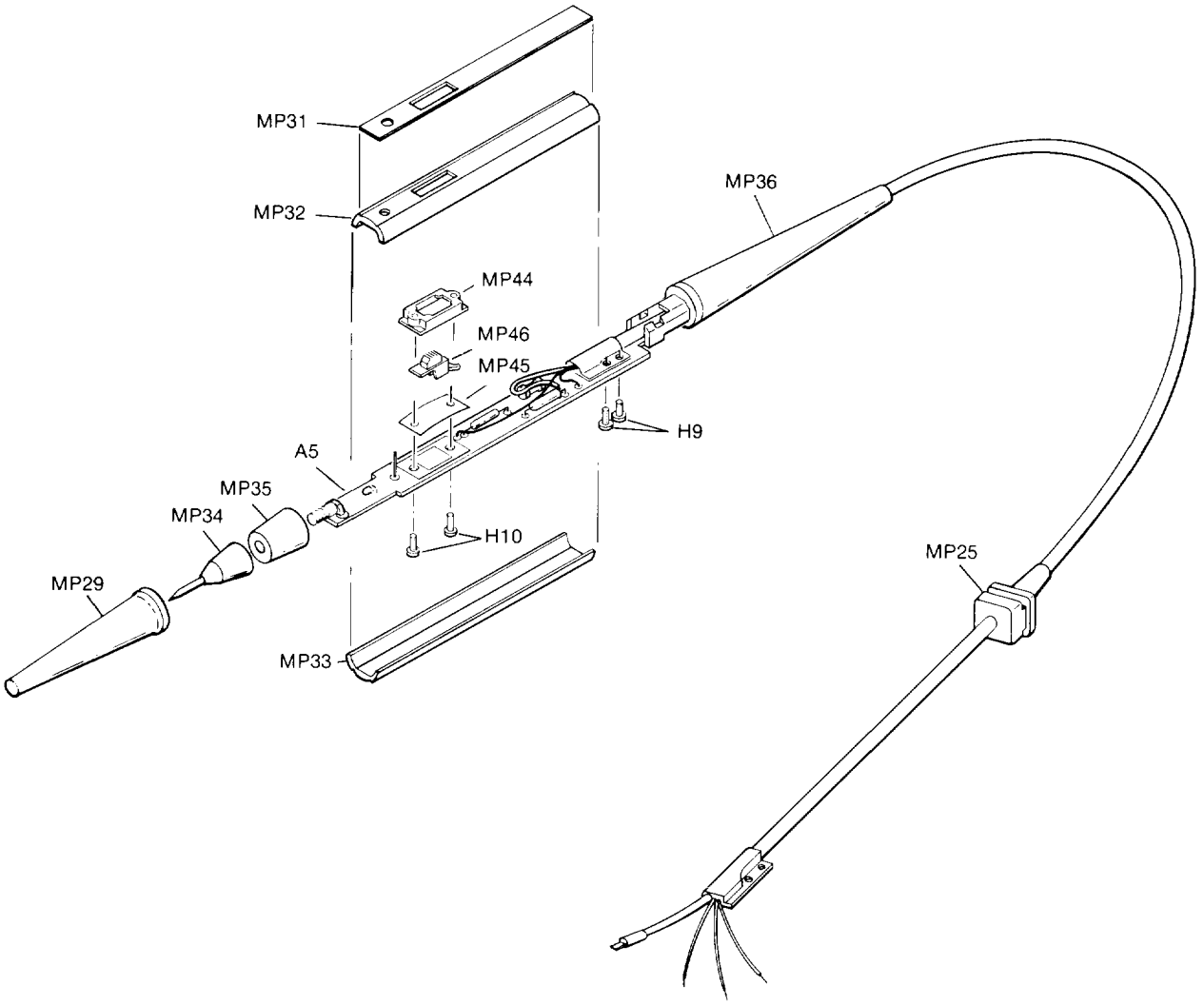
REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
MP1	5020-8816	CASTING, FRONT FRAME	1
MP15	5001-0439	TRIM, FRONT SIDE	2
MP17	05005-00009	SUBPANEL-FRONT	1
MP18	05005-00010	DRESS PANEL	1
MP19	05005-20207	WINDOW-FRONT PANEL	1
MP20	05005-40008	BOOT-POD CABLE	1
MP22	0400-0005	GROMMET-RUBBER	1
MP25	05005-40009	BOOT-PROBE CABLE	1
MP47	1460-1942	CRADLE-PROBE	1
H3	0515-0212	SCREW-MACH M3.5×0.6 6MM-LG	4
H4	0515-0218	SCREW-MACH M3.5×0.6 6MM-LG PAN HEAD	4
H7	0515-0225	SCREW-MACH M3.5×0.6 10MM-LG	6
H8	2200-0140	SCREW-MACH 4-40 .25LG	2
A4	05005-60009	DISPLAY ASSEMBLY	1
W1	05005-60101	CABLE ASSEMBLY-POWER	1

Figure 6-3. Cabinet Parts and Hardware (Front Panel)



REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
MP3	5020-8816	CASTING, REAR	1
MP16	05005-00008	PANEL-REAR	1
MP49	7122-0097	PLATE, SERIAL	1
MP50	7121-2527	LABEL, METRIC/IN	1
MP51	7121-4442	LABEL, LINE POWER MODULE	1
MP52	7121-4555	LABEL, MES. 003/80	1
A7	0960-0444	POWER LINE MODULE	1
A7F1	2110-0202	FUSE, .5A 250V (115V OPERATION)	1
	or		
	2110-0201	FUSE, .25A 250V TD (220V OPERATION)	1
A9	05005-60010	HP-IB INTERFACE ASSEMBLY	1
A9J2	1251-3283	CONN - 24 PIN	1
A9S1	3101-1973	SW:DIP 7 SPST SL	1
B1	05005-20210	FAN	1
H3	0515-0212	SCREW-MACH M3.5X0.5 6MM-LG PAN HEAD	8
H12	0380-1270	STANDOFF, 3.5MM	2

Figure 6-4. Cabinet Parts and Hardware (Rear Panel)

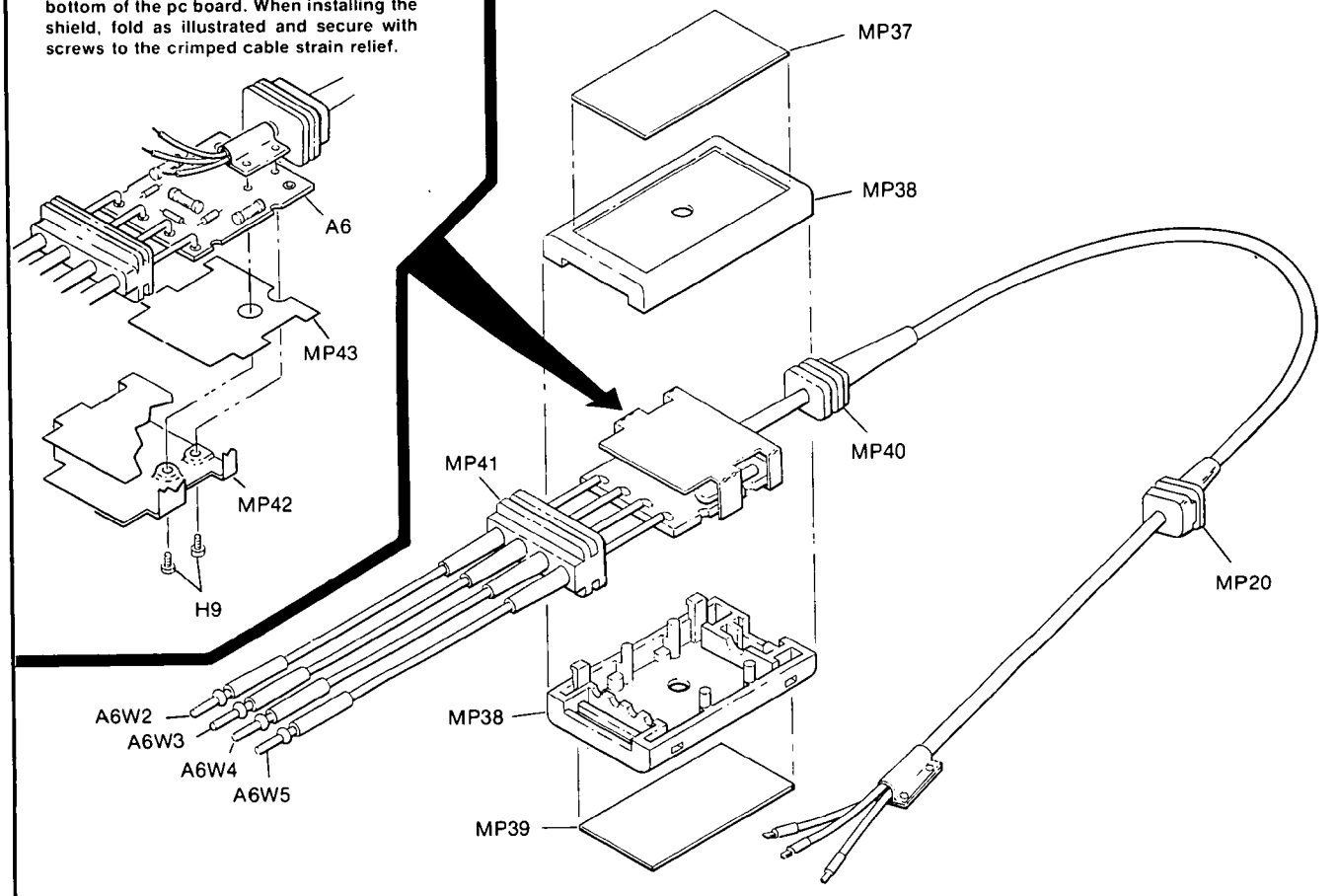


REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
	05005-60120	DATA PROBE AND CABLE ASSEMBLY	
	05005-60125	CABLE ASSEMBLY ONLY	
MP25	05005-40009	BOOT, PROBE CABLE	1
MP29	00547-40005	PROBE TIP COVER	1
MP31	7121-2701	LABEL, PROBE TIP W/GROUND & SWITCH HOLE	1
MP32	05005-20208	PROBE BODY, TOP	1
MP33	05005-20209	PROBE BODY, BOTTOM	1
MP34	5060-0418	PROBE PIN TIP ASSEMBLY	1
MP35	00546-40002	PROBE LAMP WINDOW, RED PLASTIC	1
MP36	00547-40003	BOOT, STRAIN RELIEF	1
MP44	00546-40003	RETAINER-SWITCH	1
MP45	00546-00002	CONTACT-SWITCH	1
MP46	00546-40004	BUTTON-SWITCH	1
H9	0624-0276	SCREW, TAPPING 2-32 .188 IN-LG PAN HEAD POZI	2
H10	0624-0340	SCREW-TAPPING 0-42, .188 IN-LG PAN-HD	2
A5	05005-60008	BOARD ASSEMBLY	1

Figure 6-5. Cabinet Parts and Hardware (Data Probe)

CAUTION

The Timing Pod metal shield must be installed properly. The shield has an insulated plane, which must be positioned against the bottom of the pc board. When installing the shield, fold as illustrated and secure with screws to the crimped cable strain relief.



REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
	05005-60124	TIMING POD AND CABLE ASSEMBLY	
	05005-60126	CABLE ASSEMBLY ONLY	
MP20	05005-40008	BOOT, CABLE TO FRONT PANEL	1
MP37	7121-2702	LABEL, TOP (LEFT JUSTIFIED)	1
MP38	05005-40001	POD, COVER HALF	2
MP39	7121-2703	LABEL, BOTTOM (RIGHT JUSTIFIED)	1
MP40	05005-40010	BOOT, CABLE TO POD	1
MP41	05005-40011	BOOT, TIMING LEADS TO POD	1
MP42	05005-00005	SHIELD, METAL	1
MP43	05005-00006	INSULATOR, FOR METAL SHIELD	1
H9	0624-0276	SCREW TAPPING 2-32 .188 IN-LG PAN HEAD POZI	2
A6	05005-60013	BOARD ASSEMBLY—TIMING POD	1
A6W2	05005-60112	POD LEAD, START GREEN.	1
A6W3	05005-60113	POD LEAD, STOP/QUAL RED	1
A6W4	05005-60114	POD LEAD, CLOCK Yellow	1
A6W5	05005-60115	POD LEAD, GROUND BLACK	1

Figure 6-6. Cabinet Parts and Hardware (Timing Pod)

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	05005-60011	0	1	MAIN ASSEMBLY (SERIES 2224)	28480	05005-60011
A1C1	0180-0374	3	3	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A1C2	0160-4557	0	16	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C3	0160-0576	5	8	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C4	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C5	0160-4554	7	31	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C6	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C7	0121-0061	1	1	CAPACITOR-V TRMR-CER 5.5-18PF 350V	52763	304322 5.5/18PF NPO
A1C8	0121-0114	5	3	CAPACITOR-V TRMR-CER 7-25PF 350V PC-MTG	52763	304322 7/25PF N300
A1C9	0121-0114	5		CAPACITOR-V TRMR-CER 7-25PF 350V PC-MTG	52763	304322 7/25PF N300
A1C10	0121-0114	5		CAPACITOR-V TRMR-CER 7-25PF 350V PC-MTG	52763	304322 7/25PF N300
A1C11	0160-3879	7	6	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C13	0160-3876	4	4	CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A1C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C15	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A1C16	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C17	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A1C18	0180-0410	6	1	CAPACITOR-FXD 1UF+-20% 35VDC TA	28480	0180-0410
A1C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C20	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A1C21	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C22	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C23	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C24	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C25	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C26	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C27	0180-2662	6	1	CAPACITOR-FXD 10UF+-10% 10VDC TA	25088	D4R7GS1A10K
A1C28	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C29	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C30	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C31	0180-0116	1	6	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A1C32	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C33				NOT ASSIGNED		
A1C34	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1C35	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C36	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C37	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C38	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C39	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1C40	0180-1701	2	1	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A1C41	0180-0197	0	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1C42	0180-2988	9	1	CAPACITOR-FXD 820UF+75-10% 40VDC AL	56289	39DX827G040GJ6
A1C43	0180-2811	7	1	CAPACITOR-FXD 10UF+-20% 35VDC TA	28480	0180-2811
A1C44	0180-2815	1	1	CAPACITOR-FXD 100UF+-20% 10VDC TA	28480	0180-2815
A1C45	0180-2414	6	1	CAPACITOR-FXD 2200UF+75-10% 40VDC AL	56289	36D292G040AA2A
A1C46	0180-2827	5	2	CAPACITOR-FXD 47UF+100-10% 40VDC AL	28480	0180-2827
A1C47	0180-2892	4	1	CAPACITOR-FXD 2200UF+75-10% 16VDC AL	28480	0180-2892
A1C48	0180-2827	5		CAPACITOR-FXD 47UF+100-10% 40VDC AL	28480	0180-2827
A1C49	0160-0572	1	1	CAPACITOR-FXD 2200PF +-20% 100VDC CER	28480	0160-0572
A1C50	0160-0573	2	1	CAPACITOR-FXD 4700PF +-20% 100VDC CER	28480	0160-0573
A1C51	0140-0207	7	1	CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
A1CR1	1901-0033	2	3	DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A1CR2	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A1CR3	1901-0731	7	4	DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR4	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR5	1906-0069	4	1	DIODE-FW BRDG 400V 1A	28480	1906-0069
A1CR6	1906-0096	7	1	DIODE-FW BRDG 200V 2A	04713	MDA202
A1CR7	1901-1086	7	1	DIODE-PWR RECT 50V 5A 200NS	04713	MR820
A1CR8	1902-0522	6	1	DIODE-ZNR 1N5340B 6V 5% PD=5W IR=1UA	04713	1N5340B
A1F1	2110-0003	0	1	FUSE 3A 250V NTD 1.25X.25 UL	75915	312003
A1J1	1251-6067	5	3	CONNECTOR 60-PIN M POST TYPE	28480	1251-6067
A1J2				NOT ASSIGNED		
A1J3	1251-5385	8	1	CONNECTOR 4-PIN M POST TYPE	28480	1251-5385
A1K1	0490-1220	7	2	RELAY-REED 1A 500MA 250VDC 5VDC-COIL	28480	0490-1220
A1K2	0490-1219	4	2	RELAY-REED 1C 500MA 250VDC 5VDC-COIL	28480	0490-1219
A1L1	9100-2276	9	1	INDUCTOR RF-CH-MLD 100UH 10% .105DX.26LG	28480	9100-2276
A1L2	9100-3017	8	1	300 MH AT 5 AMP DC	28480	9100-3017

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1Q1	1854-0215	1	3	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q2	1853-0363	8	1	TRANSISTOR PNP SI PD=50W FT=20MHZ	03508	X45H281
A1R1	0698-6360	6	4	RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A1R2	0698-7207	2	3	RESISTOR 61.9 1% .05W F TC=0+-100	24546	C3-1/8-TO-61R9-F
A1R3	0698-7227	6	3	RESISTOR 422 1% .05W F TC=0+-100	24546	C3-1/8-TO-422R-F
A1R4	0698-6630	3	8	RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R5	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R6	0698-0084	9	5	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A1R7	0757-0397	3	1	RESISTOR 68.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-68R1-F
A1R8	0698-6360	6		RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A1R9	0698-7210	7	1	RESISTOR 82.5 1% .05W F TC=0+-100	24546	C3-1/8-TO-82R5-F
A1R10	0698-6360	6		RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A1R11	0698-7227	6		RESISTOR 422 1% .05W F TC=0+-100	24546	C3-1/8-TO-422R-F
A1R12	0698-7207	2		RESISTOR 61.9 1% .05W F TC=0+-100	24546	C3-1/8-TO-61R9-F
A1R13	0698-7227	6		RESISTOR 422 1% .05W F TC=0+-100	24546	C3-1/8-TO-422R-F
A1R14	0698-7207	2		RESISTOR 61.9 1% .05W F TC=0+-100	24546	C3-1/8-TO-61R9-F
A1R15	0698-6360	6		RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A1R16	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R17	0698-6619	8	4	RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A1R18	0698-6348	0	4	RESISTOR 3K .1% .125W F TC=0+-25	28480	0698-6348
A1R19	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A1R20	0698-6413	0	4	RESISTOR 6.5K .1% .125W F TC=0+-25	28480	0698-6413
A1R21	0698-6413	0		RESISTOR 6.5K .1% .125W F TC=0+-25	28480	0698-6413
A1R22	0698-6348	0		RESISTOR 3K .1% .125W F TC=0+-25	28480	0698-6348
A1R23	0698-6413	0		RESISTOR 6.5K .1% .125W F TC=0+-25	28480	0698-6413
A1R24	0698-6413	0		RESISTOR 6.5K .1% .125W F TC=0+-25	28480	0698-6413
A1R25	1810-0374	1	1	NETWORK-RES 8-SIP1.0K OHM X 4	01121	208B102
A1R26	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R27	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A1R28	0698-6348	0		RESISTOR 3K .1% .125W F TC=0+-25	28480	0698-6348
A1R29	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A1R30	0698-6348	0		RESISTOR 3K .1% .125W F TC=0+-25	28480	0698-6348
A1R31	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R32	0698-3989	9	8	RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R33	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R34	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R35	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R36	1810-0273	9	1	NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1R37	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R38	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R39	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R40	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R41	0757-0280	3	10	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R42	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A1R43				NOT ASSIGNED		
A1R44	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R45	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R46	0698-3989	9		RESISTOR 3.84K .1% .125W F TC=0+-25	28480	0698-3989
A1R47	0698-3988	8	2	RESISTOR 42K .1% .125W F TC=0+-25	28480	0698-3988
A1R48	0698-3988	8		RESISTOR 42K .1% .125W F TC=0+-25	28480	0698-3988
A1R49	0698-3987	7	1	RESISTOR 70K .1% .125W F TC=0+-25	28480	0698-3987
A1R50	0698-3959	3	1	RESISTOR 80K .1% .25W F TC=0+-25	28480	0698-3959
A1R51	0698-6977	1	1	RESISTOR 30K .1% .125W F TC=0+-25	28480	0698-6977
A1R52	0811-3114	4	2	RESISTOR 75 3% 5W PW TC=0+-20	28480	0811-3114
A1R53	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R54	0757-0419	0	1	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A1R55	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A1R56				NOT ASSIGNED		
A1R57	0811-3114	4		RESISTOR 75 3% 5W PW TC=0+-20	28480	0811-3114
A1R58	0811-3288	3	1	RESISTOR .025 10% 2W PW TC=0+-180	28480	0811-3288
A1R59	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R60	0757-0199	3	1	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A1R61	0698-5210	1	1	RESISTOR 30K .5% .125W F TC=0+-100	24546	C4-1/8-T0-3002-D
A1R62	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R63	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R64	0698-4002	9	1	RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5001-F
A1R65	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R66	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1S1	3101-0488	7	1	SWITCH-SL 3-SPDT DIP-SLIDE-ASSY .1A	28480	3101-0488
A1T1	9100-0465	4	1	TRANSFORMER-POWER 100/120/220/240V	28480	9100-0465
A1TP1	1251-4707	6	10	CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP2	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP3	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP4	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP5	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1TP6	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP7	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP8	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP9	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1TP10	1251-4707	6		CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4707
A1U1	1826-0659	8	4	IC CONV 8-B-D/A 24-DIP-P PKG	34335	AM6081PC
A1U2	1820-1281	2	1	IC DCDR TTL LS 2 TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A1U3	1820-0998	6	1	IC MUXR/DATA-SEL TTL S 4-TO-1-LINE DUAL	01295	SN74S153N
A1U4	1826-0659	8		IC CONV 8 B-D/A 24-DIP-P PKG	34335	AM6081PC
A1U5	1820-1639	4	1	IC GATE TTL S EXCL-OR/NOR QUAD 2-INP	01295	SN74S135N
A1U6	1826-0630	5	1	IC COMPARATOR HS	28480	1826-0630
A1U7	1826-0659	8		IC CONV 8-B D/A 24 DIP-P PKG	34335	AM6081PC
A1U8	1820-1453	0	4	IC CNTR TTL S BIN SYNCHRO POS EDGE-TRIG	01295	SN74S163N
A1U9	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE TRIG	01295	SN74S163N
A1U10	1820-2691	0	1	IC FF TTL F D-TYPE POS-EDGE-TRIG	07263	74F74PC
A1U11	1820-1052	5	3	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U12	1820-1052	5		IC XLTR ECL ECL-TO TTL QUAD 2-INP	04713	MC10125L
A1U13	1826-0659	8		IC CONV 8 B D/A 24-DIP-P PKG	34335	AM6081PC
A1U14	1826-0522	4	1	IC OP AMP LOW-BIAS H-IMPD QUAD 14-DIP-P	01295	TL074CN
A1U15	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
A1U16	1820-1319	7	1	IC MUXR/DATA-SEL TTL S 8-TO 1-LINE 8-INP	01295	SN74S151N
A1U17	1820-0694	9	1	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
A1U18	1820-0629	0	2	IC FF TTL S J K NEG EDGE TRIG	01295	SN74S112N
A1U19	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS EDGE-TRIG	01295	SN74S163N
A1U20	1820-0629	0		IC FF TTL S J K NEG-EDGE-TRIG	01295	SN74S112N
A1U21	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U22	1820-1015	0	1	IC MUXR/DATA SEL TTL S 2-TO-1 LINE QUAD	01295	SN74S158N
A1U23	1826-0038	7	1	IC OP AMP SPCL TO-99 PKG	04713	MC1436G
A1U24	1DH3-0501	7	1	IC TTL CMOS PRB IC	28480	1DH3-0501
A1U25	1826-0565	5	1	IC-TL494	28480	1826-0565
A1U26	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1VR1	1826-0221	0	1	IC V RGLTR TO-220	04713	MC7912CT
A1VR2	1826-0215	2	1	IC V RGLTR TO-220	04713	MC7905.2CT
A1VR3	1826-0147	9	1	IC 7812 V RGLTR TO-220	04713	MC7812CP
A1W1	05005-60105	3	1	CABLE ASSEMBLY-BLACK JUMPER	28480	05005-60105
A1W2	05005-60117	7	1	CABLE ASSEMBLY-RED JUMPER	28480	05005-60117
A1W3	05005-60118	8	1	CABLE ASSEMBLY-GREEN JUMPER	28480	05005-60118
A1W4	05005-60121	3	1	CABLE ASSEMBLY-DC JUMPER	28480	05005-60121
				A1 MISCELLANEOUS PARTS		
H11	0624-0078	6	5	SCREW-TPG 6-32 .375-IN-LG PAN-HD-POZI	28480	0624-0078
MP21	0380-0630	8	8	SPACER-SNAP-IN .75 IN LG; .31 IN A/F	28480	0380-0630
MP23	5040-7721	7	6	HINGE-FULL	28480	5040-7721
MP28	1400-0493	6	1	CABLE TIE .062 1.25-DIA .14-WD NYL	06383	PLT1.5 MP8
	0340-0060	4	3	TERMINAL-STUD SPCL-FDTHRU PRESS-MTG	98291	011-6809 000 209
	1205-0349	7	4	HEAT SINK SGL PLSTC-PWR-CS	13103	6025B TT
	2110-0269	0	2	FUSEHOLDER-CLIP TYPE.25D-FUSE	28480	2110-0269
	0515-0406	3	4	SCREW MACH M3 X 0.5 8MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
	2190-0011	8	4	WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
	0535-0004	9	4	NUT-HEX DBL CHAM M3 X 0.5 2.4MM THK	00000	ORDER BY DESCRIPTION

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	05005-60002	9	1	DVM ASSEMBLY (SERIES 2324)	28480	05005-60002
A2C1	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A2C2	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A2C3	0180-0229	7	4	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A2C4	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A2C5	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A2C6	0160-5027	1	1	CAPACITOR-FXD 1200PF +-20% 400VDC POLYP	28480	0160-5027
A2C7	0160-5438	8	1	CAPACITOR-FXD 1.0UF +-10% 80VDC POLYE	28480	0160-5438
A2C8	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A2C9	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A2C10	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A2C11	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A2C12	0180-2617	1	3	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	25088	D6R8GS1B35K
A2C13	0180-2617	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	25088	D6R8GS1B35K
A2C14	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A2C15	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A2C16	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A2C17	0180-2617	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	25088	D6R8GS1B35K
A2C18	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A2C19	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A2CR1	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A2CR2	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A2CR3	1901-0376	6	4	DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A2CR4	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A2CR5	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A2CR6	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A2CR7	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A2J1	1251-6067	5		CONNECTOR 60-PIN M POST TYPE	28480	1251-6067
A2J2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A2J3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A2J4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A2K1	0490-1219	4		RELAY-REED 1C 500MA 250VDC 5VDC-COIL	28480	0490-1219
A2K2	0490-1220	7		RELAY-REED 1A 500MA 250VDC 5VDC-COIL	28480	0490-1220
A2L1	9100-1788	6	2	CHOKE-WIDE BAND ZMAX=680 OHM@ 100 MHZ	02114	VK200 20/4B
A2L2	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHM@ 100 MHZ	02114	VK200 20/4B
A2Q1				NOT ASSIGNED		
A2Q2				NOT ASSIGNED		
A2Q3	1855-0402	0	2	TRANSISTOR J-FET 2N5115 P-CHAN D-MODE	17856	2N5115
A2Q4	1855-0402	0		TRANSISTOR J-FET 2N5115 P-CHAN D-MODE	17856	2N5115
A2Q5	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A2Q6	1853-0036	2	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A2R1	0698-6369	5	1	RESISTOR 1M .1% .25W F TC=0+-25	28480	0698-6369
A2R2	2100-3161	6	1	RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TRN	02111	43P203
A2R3	0757-0200	7	1	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A2R4	0698-3986	6	4	RESISTOR 89K .1% .125W F TC=0+-25	28480	0698-3986
A2R5	0699-0724	6	1	RESISTOR 10M .1% 1W F TC=0+-25	28480	0699-0724
A2R6	0698-3960	6	1	RESISTOR 1.1M 1% .125W F TC=0+-100	28480	0698-3960
A2R7	0757-0465	6	1	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A2R8	0698-6612	1	2	RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A2R9	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A2R10	0698-6625	6	1	RESISTOR 6K .1% .125W F TC=0+-25	28480	0698-6625
A2R11	0757-0442	9	7	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R12	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R13	0699-0283	2	1	RESISTOR 81.92K .1% .125W F TC=0+-25	28480	0699-0283
A2R14	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A2R15	0698-3158	4	1	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
A2R16	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A2R17	0698-6358	2	1	RESISTOR 100K .1% .125W F TC=0+-25	28480	0698-6358
A2R18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R19	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R20	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A2R21	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R22	0757-0458	7	1	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A2R23	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R25	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A2R26	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A2R27	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A2R28	0757-0440	7	1	RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A2R29	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R30	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2R31	0698-0084	2		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A2R32	0757-0447	4	1	RESISTOR 16.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1622 F
A2R33	0698-3444	1	1	RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R F
A2R34	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R35	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A2R36	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2TP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM BSC-SZ SQ	28480	1251-0600
A2TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM BSC-SZ SQ	28480	1251-0600
A2TP3	1251-4303	6	1	CONNECTOR 15-PIN M POST TYPE	28480	1251-4303
A2TP4	1251-4303	6		CONNECTOR 15-PIN M POST TYPE	28480	1251-4303
A2TP5	1251-4303	6		CONNECTOR 15-PIN M POST TYPE	28480	1251-4303
A2TP6	1251-4303	6		CONNECTOR 15-PIN M POST TYPE	28480	1251-4303
A2TP7	1251-4303	6		CONNECTOR 15-PIN M POST TYPE	28480	1251-4303
A2U1	1826-0650	9	1	IC-AD 584KH	28480	1826-0650
A2U2	1826-0658	7	1	IC SWITCH 16-DIP-P PKG	3L585	C0221B8E
A2U3	1826-0543	9	1	IC OP AMP LOW-DRIFT TO-99 PKG	06665	OP-07CJ
A2U4	1826-0588	2	1	IC CONV 16-DIP P PKG	17856	LD120CJ
A2U5	1820-2326	8	1	IC XLTR CMOS TTL-TO-MOS HEX	04713	MC14504BCP
A2U6	1826-0412	1	1	IC COMPARATOR PRCN DUAL 8-DIP-P PKG	27014	LM393N
A2U7	1826-0587	1	1	IC CONV 18-DIP-P PKG	17856	LD121CJ
A2U8	1820-1430	3	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A2U9	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A2U10	1826-0909	1	1	IC OP AMP PRCN TO-99 PKG	27014	LM11CH
				A2 MISCELLANEOUS PARTS		
H11	0624-0078	6		SCREW-TPG 6-32 .375-IN-LG PAN-HD-POZI	28480	0624-0078
MP21	0380-0630	8		SPACER-SNAP-IN .75 IN LG; .31 IN A/F	28480	0380-0630
MP23	5040-7721	7		HINGE-FULL	28480	5040-7721
	3050-0016	8	1	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0016

See introduction to this section for ordering information
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Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	05005-60012	1	1	MICROPROCESSOR ASSEMBLY (SERIES 2204)	28480	05005-60012
A3C1	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A3C2	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A3C3	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C4	0180-2816	2	2	CAPACITOR-FXD 68UF+-20% 10VDC TA	28480	0180-2816
A3C5	0180-2816	2		CAPACITOR-FXD 68UF+-20% 10VDC TA	28480	0180-2816
A3C6	0160-0127	2	2	CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-0127
A3C7	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A3C8	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C9	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C10	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A3C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C12	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A3C13	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C14	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C15	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A3C16	0180-0230	0	2	CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A3CR1	1901-0518	8	1	DIODE-SM SIG SCHOTTKY	28480	1901-0518
A3CR2	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3J1	1251-6067	5		CONNECTOR 60-PIN M POST TYPE	28480	1251-6067
A3Q1	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3R1	0698-8812	7	1	RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812
A3R2	0698-7244	7	3	RESISTOR 2.15K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2151-F
A3R3	0698-7244	7		RESISTOR 2.15K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2151-F
A3R4	1810-0369	4	3	NETWORK-RES 6-SIP100.0K OHM X 5	11236	750-61-R100K
A3R5	0698-7252	7	2	RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-F
A3R6	0698-7257	2	2	RESISTOR 7.5K 1% .05W F TC=0+-100	24546	C3-1/8-T0-7501-F
A3R7	0698-7257	2		RESISTOR 7.5K 1% .05W F TC=0+-100	24546	C3-1/8-T0-7501-F
A3R8	0698-7252	7		RESISTOR 4.64K 1% .05W F TC=0+-100	24546	C3-1/8-T0-4641-F
A3R9	0698-7231	2	22	RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-F
A3R10	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-F
A3R11	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-F
A3R12	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-F
A3R13	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-F
A3R14	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-F
A3R15	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-T0-619R-F
A3R16	0698-7246	7	1	RESISTOR 2.61K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2611-F
A3R17	0698-7244	7		RESISTOR 2.15K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2151-F
A3R18	0698-7233	4	1	RESISTOR 750 1% .05W F TC=0+-100	24546	C3-1/8-T0-750R-F
A3R19	0698-7220	9	1	RESISTOR 215 1% .05W F TC=0+-100	24546	C3-1/8-T0-215R-F
A3R20	0698-7236	7	3	RESISTOR 1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1001-F
A3R21	1810-0368	3	3	NETWORK-RES 6-SIP10.0K OHM X 5	01121	206A103
A3R22				NOT ASSIGNED		
A3R23	0698-7260	7	4	RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-F
A3R24	0698-7260	7		RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-F
A3R25	0698-7270	9	1	RESISTOR 26.1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-2612-F
A3R26	0698-7236	7		RESISTOR 1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1001-F
A3R27	1810-0206	8	2	NETWORK-RES 8-SIP10.0K OHM X 7	01121	208A103
A3R28	0698-7260	7		RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1002-F
A3R29	0698-7284	5	2	RESISTOR 100K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1003-F
A3S1	3100-3364	2	2	SWITCH-ROTARY 16 PIN DIP 4PDT	28480	3100-3364
A3S2	3100-3364	2		SWITCH-ROTARY 16 PIN DIP 4PDT	28480	3100-3364
A3TP1				NOT ASSIGNED		
A3TP2-A3TP16	1251-4303	8	1	CONNECTOR 15-PIN M POST TYPE	28480	1251-4303
A3U1	1813-0139	2	1	IC OSC HYBRID	34344	K1100A-10.0MHZ
A3U2	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A3U3	1820-2309	7	2	IC ENCDR CMOS	27014	MM74C923N
A3U4	1818-1542	3	1	IC-ROM W/16 I/O LINES, (2KX8), USE	28480	1818-1542
A3U5	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U6	1820-2132	4	1	IC DRVR CMOS LED DRVR	32293	ICM7218A
A3U7	1820-0174	0	2	IC INV TTL HEX	01295	SN7404N
A3U8	1818-0696	6	1	IC NMOS 2048 (2K) STAT RAM 400-NS	28480	1818-0696
A3U9	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U10	1820-0174	0		IC INV TTL HEX	01295	SN7404N

See introduction to this section for ordering information
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Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U11	1818-1543	4	1	IC-ROM W/16 I/O LINES, (2KX8), USE	28480	1818-1543
A3U12	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U13	1818-1544	5	1	IC-ROM W/16 I/O LINES, (2KX8), USE	28480	1818-1544
A3U14	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
A3U15	1820-1245	8	1	IC DCDR TTL LS 2 TO 4-LINE DUAL 2-INP	01295	SN74LS155N
A3U16	1820-2074	3	2	IC MICPROC NMOS 8-BIT	34649	P8085
A3XS1	1200-0607	0	2	SOCKET-IC 16 CONT DIP DIP-SLDR	28480	1200-0607
A3XS2	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A3XU4	1200-0654	7	7	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3XU6	1200-0567	1	2	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU8	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3XU11	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3XU13	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3XU16	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
				A3 MISCELLANEOUS PARTS		
H11	0624-0078	6		SCREW-TPG 6-32 .325-IN-LG PAN-HD-POZI	28480	0624-0078
MP21	0380-0630	8		SPACER-SNAP-IN .75 IN LG; .31 IN A/F	28480	0380-0630
MP23	5040-7721	7		HINGE-HALF	28480	5040-7721

See introduction to this section for ordering information
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Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	05005-60009	6	1	DISPLAY ASSEMBLY (SERIES 2304)	28480	05005-60009
A4DS1	1990-0730	3	6	DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611
A4DS2	1990-0730	3		DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611
A4DS3	1990-0730	3		DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611
A4DS4	1990-0730	3		DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611
A4DS5	1990-0730	3		DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611
A4DS6	1990-0730	3		DISPLAY-NUM-SEG 1-CHAR .3-H RED	28480	5082-7611
A4DS7	1990-0547	0	24	LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1995	4	2	STANDOFF-LED .177-IN-WD .177-IN-LG	28480	4040-1995
A4DS8	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1995	4		STANDOFF-LED .177-IN-WD .177-IN-LG	28480	4040-1995
A4DS9	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5	23	STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A4DS10	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A4DS11	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A4DS12	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A4DS13	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS14	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS15	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS16	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS17	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS18	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS19	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS20	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS21	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS22	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS23	1990-0487	7	1	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4584
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS24	1990-0665	3	10	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS25	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS26	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS27	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS28	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS29	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS30	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF SPACER (LED)	28480	4040-1615
A4DS31	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A4DS32	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A4DS33	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A4DS34	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A4DS35	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A4DS36	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A4DS37	1990-0547	0		LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
	4040-1615	5		STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A4DS38	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS39	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS40	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS41	1990-0665	3		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	1990-0665
A4DS42	0960-0553	4	1	AUDIO TRANSDUCER 2-10VDC; 75-95DB SOUND	28480	0960-0553
A4S1	5060-9436	7	21	PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1845	6	2	KEY CAP SPECIAL	28480	5041-1845
A4S2	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0252	7	11	KEY CAP QUARTER GY-LIT	28480	5041-0252
A4S3	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0252	7		KEY CAP QUARTER GY-LIT	28480	5041-0252

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4S4	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0252	7		KEY CAP QUARTER GY-LIT	28480	5041-0252
A4S5	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0252	7		KEY CAP QUARTER GY-LIT	28480	5041-0252
A4S6	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0252	7		KEY CAP QUARTER GY-LIT	28480	5041-0252
A4S7	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0252	7		KEY CAP QUARTER GY-LIT	28480	5041-0252
A4S8	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0243	7	9	*U.K. CAP-S.M., GRAY	28480	5041-0243
A4S9	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0243	6		*U.K. CAP-S.M., GRAY	28480	5041-0243
A4S10	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0243	6		*U.K. CAP-S.M., GRAY	28480	5041-0243
A4S11	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1845	6		KEY CAP SPECIAL	28480	5041-1845
A4S12	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0243	6		*U.K. CAP-S.M., GRAY	28480	5041-0243
A4S13	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0252	7		KEY CAP QUARTER GY-LIT	28480	5041-0252
A4S14	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0252	7		KEY CAP QUARTER GY-LIT	28480	5041-0252
A4S15	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0252	7		KEY CAP QUARTER GY-LIT	28480	5041-0252
A4S16	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0252	7		KEY CAP QUARTER GY-LIT	28480	5041-0252
A4S17	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0243	6		*U.K. CAP-S.M., GRAY	28480	5041-0243
A4S18	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0243	6		*U.K. CAP-S.M., GRAY	28480	5041-0243
A4S19	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0243	6		*U.K. CAP-S.M., GRAY	28480	5041-0243
A4S20	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0243	6		*U.K. CAP-S.M., GRAY	28480	5041-0243
A4S21	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-0243	6		*U.K. CAP-S.M., GRAY	28480	5041-0243
A4W1	05005-60122	4	1	CABLE ASSEMBLY-DISPLAY	28480	05005-60122
A4XDS1	1200-0424	9	6	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
A4XDS2	1200-0424	9		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
A4XDS3	1200-0424	9		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
A4XDS4	1200-0424	9		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
A4XDS5	1200-0424	9		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
A4XDS6	1200-0424	9		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0424
				A4 MISCELLANEOUS PARTS		
MP22	0400-0005	5	1	GROMMET-RND .438 IN-ID .562-IN-GRV-OD	28480	0400-0005

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5				PROBE ASSEMBLY		
A5W1	8120-3505	0	1	ER DIVISION	28480	8120-3505
A5A1	05005-60000	5	1	BOARD ASSEMBLY-PROBE (SERIES 2324)	28480	05005-60008
A5A1C1	0160-2255	1	1	CAPACITOR-FXD 0.2PF +-.25PF 500VDC CER	28480	0160-2255
A5A1DS1	2140-0346	7	1	LAMP-INCAND 7210 5VDC 30MA T-1-BULB	1F556	7210
A5A1R1	0698-3985	5	1	RESISTOR 89.6K .1% .25W F TC=0+-25	28480	0698-3985
A5A1R2	0698-7496	1	1	RESISTOR 20K .1% .25W F TC=0+-25	28480	0698-7496
				A5 MISCELLANEOUS PARTS		
H9	0624-0276	6	8	SCREW-TPG 2-32 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H10	0624-0340	5	1	SCREW-TPG 0-42 .188-IN-LG BDG-HD-SLT STL	00000	ORDER BY DESCRIPTION
MP25	05005-40009	4	1	BOOT-PROBE CABLE	28480	05005-40009
MP29	00547-40005	5	1	COVER-TIP	28480	00547-40005
MP32	05005-20208	3	1	BODY-BOTTOM HALF	28480	05005-20208
MP33	05005-20209	4	1	BODY-TOP HALF	28480	05005-20209
MP34	5060-0418	7	1	PIN TIP ASSY	28480	5060-0418
MP35	00546-40002	1	1	WINDOW	28480	00546-40002
MP36	00547-40003	3	1	BOOT-STRAIN RELIEF	28480	00547-40003
MP45	00546-00002	7	1	SWITCH CONTACT	28480	00546-00002
MP44	00546-40003	2	1	RETAINER-SWITCH	28480	00546-40003
MP46	00546-40004	3	1	BUTTON SWITCH	28480	00546-40004
W3	05005-60116	6	1	CABLE ASSEMBLY-PROBE GROUND	28480	05005-60116
	0362-0028	0	1	SLEEVE-METAL BRZ BLU .08-IN-OD	28480	0362-0028
	0362-0037	1	10	SLEEVE-METAL BRZ GRN .071-IN-OD	28480	0362-0037
	05005-20204	9	2	CRIMP SLEEVE-PROBE	28480	05005-20204
	0890-0732	2	70	TUBING-HS .063-D/.031-RCVD .017-WALL	28480	0890-0732
	1530-0068	6	8	TUBE SEAMLESS NI	28480	1530-0068
	1600-0506	6	1	WASHER GRD	28480	1600-0506
MP31	7121-2701	7	1	LABEL-INFORMATION 0-MM-WD 123.5-MM-LG	28480	7121-2701
				A5A1 MISCELLANEOUS PARTS		
	1251-4259	3	1	CONNECTOR-SGL CONT PIN .031-IN-BSC-SZ	28480	1251-4259
	0570-0662	9	1	STUD-PROBE TIP	28480	0570-0662

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6				POD ASSEMBLY		
A6W1	8120-3118	1	1	CABLE-SHLD 30AWG 3-CNDCT JGK-JKT	28480	8120-3118
A6W2	05005-60112	2	1	CABLE ASSEMBLY-START/ST-SP, W/G	28480	05005-60112
A6W3	05005-60113	3	1	CABLE ASSEMBLY-STOP/QUAL, W/R	28480	05005-60113
A6W4	05005-60114	4	1	CABLE ASSEMBLY-CLK, W/Y	28480	05005-60114
A6W5	05005-60115	5	1	CABLE ASSEMBLY-GND, BLACK	28480	05005-60115
A6A1	05005-60013	2	1	BOARD ASSEMBLY-POD (SERIES 2204)	28480	05005-60013
A6A1C1	0160-2254	0	3	CAPACITOR-FXD 7.5PF +-.25PF 500VDC CER	28480	0160-2254
A6A1C2	0160-2254	0		CAPACITOR-FXD 7.5PF +-.25PF 500VDC CER	28480	0160-2254
A6A1C3	0160-2254	0		CAPACITOR-FXD 7.5PF +-.25PF 500VDC CER	28480	0160-2254
A6A1R1	0698-3986	6		RESISTOR 89K .1% .125W F TC=0+-25	28480	0698-3986
A6A1R2	0698-3986	6		RESISTOR 89K .1% .125W F TC=0+-25	28480	0698-3986
A6A1R3	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A6A1R4	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A6A1R5	0698-3986	6		RESISTOR 89K .1% .125W F TC=0+-25	28480	0698-3986
A6A1R6	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
				A6 MISCELLANEOUS PARTS		
H9	0624-0276	6		SCREW-TPG 2-32 .188-IN-LG PAN-HD-POZI	00800	ORDER BY DESCRIPTION
MP20	05005-40000	3	1	BOOT-POD CABLE	28480	05005-40000
MP37	7121-2702	8	1	LABEL-INFORMATION 26-MM-WD 54-MM-LG	28480	7121-2702
MP38	05005-40001	6	2	COVER-POD	28480	05005-40001
MP39	7121-2703	9	1	LABEL-INFORMATION 26-MM-WD 54-MM-LG	28480	7121-2703
MP40	05005-40010	7	1	BOOT-POD	28480	05005-40010
MP41	05005-40011	8	1	BOOT-POD LEADS	28480	05005-40011
MP42	05005-00005	6	1	SHIELD-POD	28480	05005-00005
MP43	05005-00006	7	1	INSULATOR-POD	28480	05005-00006
	0362-0037	1		SLEEVE-METAL BRZ GRN .071-IN-OD	28480	0362-0037
	05005-20205	0	2	CRIMP-SLEEVE POD	28480	05005-20205
	0890-0732	2		TUBING-HS .063 D/.031-RCVD .017-WALL	28480	0890-0732
	1530 0068	6		TUBE SEAMLESS NI	28480	1530-0068
				5005B SIGNATURE MULTIMETER POWER INPUT, MODULE		
A7	0960-0444	2	1	LINE MODULE-UNFILTERED	28480	0960-0444
A7F1	2110-0202	1	1	FUSE .5A 250V TD 1.25X.25 UL	75915	313.500

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	05005-60007	4	1	HP-IB ASSEMBLY (SERIES 2312)		
A8C1	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C2	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C3	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C4	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A8C5	0180-2929	8	1	CAPACITOR-FXD 68UF+-10% 10VDC TA	28480	0180-2929
A8C6	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C7	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C8	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C9	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C10	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C11	0160-4795	0	1	CAPACITOR-FXD 4.7PF +-.5PF 100VDC CER	28480	0160-4795
A8C12	0160-4791	4	1	CAPACITOR-FXD 10PF +-5% 100VDC CER 0+-30	28480	0160-4791
A8C13	0180-0230	0		CAPACITOR-FXD 1UF+-20% 50VDC TA	56289	150D105X0050A2
A8C14	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C15	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C16	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C17	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C18	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C19	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C20	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C21	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C22	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C23	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C24	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A8C25	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A8C26	0160-0127	2		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-0127
A8CR1	1901-0050	3	5	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A8CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A8CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A8CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A8CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A8CR6	1906-0229	8	1	DIODE-ARRAY 50V 400MA	01295	TID133
A8J1				NOT ASSIGNED		
A8J2				NOT ASSIGNED		
A8J3	1200-0541	1	3	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A8J4	1251-7424	0	1	CONN-POST TYPE .100-PIN-SPCG 4-CONT	28480	1251-7424
A8J5	1251-4303	8		CONNECTOR 15-PIN M POST TYPE	28480	1251-4303
A8Q1	1858-0010	2	1	TRANSISTOR ARRAY 14-PIN PLSTC DIP	04713	MPQ2906
A8R1	0698-7199	1	8	RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-TO-28R7-F
A8R2	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R3	0698-7199	1		RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-TO-28R7-F
A8R4	0698-7199	1		RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-TO-28R7-F
A8R5	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R6	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R7	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R8	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R9	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R10	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R11	0757-0709	1	1	RESISTOR 68.1 1% .25W F TC=0+-100	24546	C5-1/4-TO-68R1-F
A8R12	0698-7253	0	2	RESISTOR 5.11K 1% .05W F TC=0+-100	24546	C3-1/8-TO-5111-F
A8R13	0698-7253	8		RESISTOR 5.11K 1% .05W F TC=0+-100	24546	C3-1/8-TO-5111-F
A8R14	0698-7248	1	1	RESISTOR 3.16K 1% .05W F TC=0+-100	24546	C3-1/8-TO-3161-F
A8R15	0698-7236	7		RESISTOR 1K 1% .05W F TC=0+-100	24546	C3-1/8-TO-1001-F
A8R16	0698-7199	1		RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-TO-28R7-F
A8R17	0698-7199	1		RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-TO-28R7-F
A8R18	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R19	0698-7199	1		RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-TO-28R7-F
A8R20	0698-7199	1		RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-TO-28R7-F
A8R21	0698-7199	1		RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-TO-28R7-F
A8R22	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R23	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R24	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R25	0698-7231	2		RESISTOR 619 1% .05W F TC=0+-100	24546	C3-1/8-TO-619R-F
A8R26	0698-7220	7	1	RESISTOR 464 1% .05W F TC=0+-100	24546	C3-1/8-TO-4640-F
A8R27	0698-7284	5		RESISTOR 100K 1% .05W F TC=0+-100	24546	C3-1/8-TO-1003-F
A8R28	1810-0368	3		NETWORK-RES 6-SIP10.0K OHM X 5	01121	206A103
A8R29	1810-0371	8	2	NETWORK-RES 8-SIP100.0K OHM X 7	01121	208A104
A8R30	1810-0275	1	1	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
A8R31	1810-0280	8	3	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A8R32	1810-0206	8		NETWORK-RES 8-SIP10.0K OHM X 7	01121	208A103
A8R33	0698-7260	7		RESISTOR 10K 1% .05W F TC=0+-100	24546	C3-1/8-TO-1002-F
A8R34	1810-0371	8		NETWORK-RES 8-SIP100.0K OHM X 7	01121	208A104
A8R35	1810-0368	3		NETWORK-RES 6-SIP10.0K OHM X 5	01121	206A103

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8R36	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A8R37	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A8R38	1810-0369	4		NETWORK-RES 6-SIP100.0K OHM X 5	11236	750-61-R100K
A8R39	1810-0369	4		NETWORK-RES 6-SIP100.0K OHM X 5	11236	750-61-R100K
A8S1	3101-1841	8	1	SWITCH-SL 4-1A DIP-SLIDE ASSY .1A 50VDC	28480	3101-1841
A8TP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A8TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A8U1	1820-1200	5	1	IC INV TTL LS HEX	01295	SN74LS05N
A8U2	1820-0618	7	2	IC BFR TTL NON-INV HEX	01295	SN7417N
A8U3	1820-0618	7		IC BFR TTL NON-INV HEX	01295	SN7417N
A8U4	1820-2537	3	5	IC DRVR CMOS LINE DRVR OCTL	27014	MM74C244N
A8U5	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A8U6	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A8U7	1820-2074	3		IC MICPROC NMOS 8-BIT	34649	P8085
A8U8	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A8U9	1820-2549	7	1	IC-8291A P HPIB	28480	1820-2549
A8U10	1820-2485	0	1	IC RCVR TTL LS BUS OCTL	01295	SN75160N
A8U11	1820-2216	5	2	IC FF CMOS D-TYPE POS-EDGE-TRIG OCTL	27014	MM74C374N
A8U12	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A8U13	1820-2537	3		IC DRVR CMOS LINE DRVR OCTL	27014	MM74C244N
A8U14	1820-2537	3		IC DRVR CMOS LINE DRVR OCTL	27014	MM74C244N
A8U15	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A8U16	1820-2216	5		IC FF CMOS D-TYPE POS-EDGE-TRIG OCTL	27014	MM74C374N
A8U17	1820-2483	8	1	IC RCVR TTL LS BUS OCTL	01295	SN75161N
A8U18	1820-2537	3		IC DRVR CMOS LINE DRVR OCTL	27014	MM74C244N
A8U19	1820-1266	3	1	IC BFR CMOS NON-INV HEX	07263	40097PC
A8U20	1820-2309	7		IC ENCDR CMOS	27014	MM74C923N
A8U21	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A8U22	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A8U23	1818-3161	6	1	IC NMOS 65536 (64K) ROM 250-NS 3-S	28480	1818-3161
A8U24	1818-1967	6	1	IC NMOS 8192 (8K) STAT RAM 250-NS 3-S	28480	1818-1967
A8U25	1820-2537	3		IC DRVR CMOS LINE DRVR OCTL	27014	MM74C244N
A8W1-9	1251-6524	9	1	SHUNT-DIP 9 POSITION; DUAL INLINE PKG	28480	1251-6524
A8W10	05005-60106	4	1	CABLE ASSEMBLY 34-PIN	28480	05005-60106
A8XU7	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A8XU9	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A8XU10	1200-0639	8	2	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A8XU17	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A8XU23	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A8XU24	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A8XW1-9	1200-0539	7	1	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
A8Y1	0410-1142	4	1	CRYSTAL-QUARTZ 4.00000 MHZ HC-18/U-HLDR	28480	0410-1142
				A8 MISCELLANEOUS PARTS		
MP24	5040-7787	5	2	HINGE-HALF	28480	5040-7787

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9	05005-60010	9	1	HP-IB INTERFACE ASSEMBLY (SERIES 2204)		
A9J1	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A9J2	1251-3283	1	1	CONNECTOR 24-PIN F MICRORIBBON	28480	1251-3283
A9S1	3101-1973	7	1	SWITCH-SL 7-1A DIP-SLIDE-ASSY .1A 50VDC	28480	3101-1973
A9XS1	1200-0485	2	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0485
				A9 MISCELLANEOUS PARTS		
H12	0380-1270	4	2	STANDOFF-HEX 8.89-MM-LG 7.1-MM-A/F STL	00000	ORDER BY DESCRIPTION
H13	2190-0034	5	2	WASHER-LK HLCL NO. 10 .124-IN-ID	28480	2190-0034
H14	3050-1072	8	2	WASHER-FL MTLC NO. 10 .195-IN-ID	86928	5710-40-20
H15	0360-0268	6	1	TERMINAL-SLDR LUG LK-MTG FOR-#6-SCR	28480	0360-0268
MP48	1531-0109	8	2	MACHINED PART-DRS CLEVIS	28480	1531-0109
	0361-0012	0	2	RIVET-SEMI TUBULAR	28480	0361-0012
	8150-0403	4	1	WIRE 18AWG BK 300V PVC 19X30 80C	28480	8150-0403

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				MISCELLANEOUS/CHASSIS PARTS		
B1	05005-20210	7	1	FAN-MODIFIED	28480	05005-20210
C1	0160-4281	7	2	CAPACITOR-FXD 2200PF +-20% 250VAC(RMS)	C0633	PME271Y422
C2	0160-4281	7		CAPACITOR-FXD 2200PF +-20% 250VAC(RMS)	C0633	PME271Y422
H1	2680-0172	1	2	SCREW-MACH 10-32 .375-IN-LG 100 DEG	28480	2680-0172
H2	2510-0192	6	12	SCREW-MACH 8-32 .25-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H3	0515-0212	9	9	SCREW-MACH M3.5 X 0.6 6MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H4	0515-0210	5	4	SCREW-MACH M3.5 X 0.6 6MM-LG	00000	ORDER BY DESCRIPTION
H5	0590-0639	2	1	NUT-SHMET-FLT 10-32-THD STL	28480	0590-0639
H6	0515-0413	2	4	SCREW-MACH M4 X 0.7 6MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H7	0515-0225	4	6	SCREW-MACH M3.5 X 0.6 10MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H8	2200-0140	7	2	SCREW MACH 4-40 .25-IN-LG 100 DEG	28480	2200-0140
H9	0624-0276	6		SCREW-TPG 2-32 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP1	5020-8815	0	1	CASTING, FRONT FRAME	28480	5020-8815
MP2	5020-8836	5	2	STRUT	28480	5020-8836
MP3	5020-8816	1	1	CASTING, REAR FRAME	28480	5020-8816
MP4	05005-00012	5	1	SUPPORT-PCB	28480	05005-00012
MP5	05005-00011	4	1	STRUT-TOP	28480	05005-00011
MP6	05005-00007	8	1	COVER-TOP	28480	05005-00007
MP7	5040-7219	8	1	STRAP, HANDLE, CAP-FRONT	28480	5040-7219
MP8	5040-7220	1	1	STRAP, HANDLE, CAP-REAR	28480	5040-7220
MP9	5060-9803	2	1	STRAP HANDLE	28480	5060-9803
MP10	5060-9964	6	1	COVER-BOTTOM	28480	5060-9964
MP11	5040-7201	8	2	FOOT	28480	5040-7201
MP12	5040-7222	3	2	FOOT-NONSKID	28480	5040-7222
MP13	1460-1345	5	1	TILT STAND SST	28480	1460-1345
MP14	5040-7203	0	1	TRIM:TOP 1/2	28480	5040-7203
MP15	5001-0439	8	2	TRIM, FRONT SIDE	28480	5001-0439
MP16	05005-00008	9	1	PANEL-REAR	28480	05005-00008
MP17	05005-00009	0	1	SUB PANEL-FRONT	28480	05005-00009
MP18	05005-00010	3	1	DRESS PANEL	28480	05005-00010
MP19	05005-20207	2	1	WINDOW FRONT PANEL	28480	05005-20207
MP26	1400-0249	0	1	CABLE TIE .062-.625-DIA .091-WD NYL	06383	PLT1M-8
MP27	1400-1140	2	1	CLAMP-FL-DA NYL	28480	1400-1140
MP30	10230-62101	7	5	GRABBER	28480	10230-62101
MP47	1460-1942	8	1	WIREFORM 150.2-MM-W SST PSVT	28480	1460-1942
MP49	7122-0097	2	1	PLATE-SERIAL	28480	7122-0097
MP50	7121-2527	5	2	LABEL-INFORMATION 15-MM-WD 38-MM-LG	28480	7121-2527
MP51	7121-4442	7	1	LABEL INFORMATION .21-IN-WD 2.33-IN-LG	28480	7121-4442
MP52	7121-4555	3	1	LABEL, MES .003180	28480	7121-4555
S1	3101-2080		1	SW ROCKER HP POWER		3101-2080
W1	05005-60101	9	1	CABLE ASSEMBLY-POWER (POWER SWITCH IS PART OF THIS ASSEMBLY)	28480	05005-60101
W2	05005-60104	2	1	CABLE ASSEMBLY - 60-PIN RB	28480	05005-60104
W4	8120-3466		1	CABLE ASSEMBLY 24-PIN FLAT	28480	8120-3466
	8120-1521	6	1	CABLE ASSY 18AWG 3-CNDCT JCK-JKT	28480	8120-1521
	0510-0592	0	1	RETAINER-PUSH ON TUB EXT .14-IN-DIA	28480	0510-0592
	1400-0913	5	1	SADDLE-WIRE .450 IN INSIDE HEIGHT, .437	06915	WS-2NA
	0361-0316	7	2	RIVET-BLIND	28480	0361-0316
	0362-0265	7	2	CONNECTOR-SGL CONT SKT 1.14-MM-BSC-SZ	28480	0362-0265
	0380-1370	5	2	STANDOFF-HEX 10-MM-LG M4.0 X 0.7-THD	28480	0380-1370
	0380-1489	7	2	SPACER-SNAP-IN .375 IN LG; .280 IN OD	00000	ORDER BY DESCRIPTION
	0515-0642	9	10	SCREW-MACH M3.5 X 0.6 8MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
	0624-0411	1	6	SCREW-TPG 6-19 .313-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	0890-0983	5	2	TUBING-HS .125-D/.062-RCVD .02-WALL	28480	0890-0983
	2190-0011	8		WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
	2680-0129	8	2	SCREW-MACH 10-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-8. Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
C0633	RIFA	BROMMA	
00000	ANY SATISFACTORY SUPPLIER		
01121	ALLEN-BRADLEY CO	MILWAUKEE, WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS, TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND, CA	91745
02114	FERROXCUBE CORP	SAUGERTIES, NY	12477
03508	GE CO SEMICONDUCTOR PROD DEPT	SYRACUSE, NY	13201
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX, AZ	85062
06383	PANDUIT CORP	TINLEY PARK, IL	60477
06665	PRECISION MONOLITHICS INC	SANTA CLARA, CA	95050
06915	RICHCO PLASTIC CO	CHICAGO, IL	60646
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW, CA	94042
1F556	PRECISION LAMP INC	MOUNTAIN VIEW, CA	94040
11236	CTS OF BERNE INC	BERNE, IN	46711
13103	THERMALLOY CO	DALLAS, TX	75234
16299	CORNING GL WKS ELEC CMPNT DIV	RALEIGH, NC	27604
17856	SILICONIX INC	SANTA CLARA, CA	95054
19701	MEPCO/ELECTRA CORP	MINERAL WELLS, TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD, PA	16701
25088	SIEMENS CORP	ISELIN, NJ	08830
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA, CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO, CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE, NJ	
32293	INTERSIL INC	CUPERTINO, CA	95014
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE, CA	94086
34344	MOTOROLA INC	FRANKLIN PARK, IL	60131
34649	INTEL CORP	SANTA CLARA, CA	95051
52763	STETTNER ELECTRONICS INC	CHATTANOOGA, TN	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS, MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE, SC	06226
75915	LITTELFUSE INC	DES PLAINES, IL	60016
86928	SEASTROM MFG CO	GLENDALE, CA	91201
98291	SEALECTRO CORP	MAMARONECK, NY	10544

SECTION VII
MANUAL CHANGES

7-1. INTRODUCTION

7-2. This section contains information necessary to adapt this manual to apply to older instruments.

7-3. MANUAL CHANGES

7-4. This manual applies directly to Model 5005B Signature Multimeters with serial number prefix 2324A.

7-5. As engineering changes are made, newer instruments may have serial prefix numbers higher than 2324A. The manuals for these instruments will be supplied with yellow "MANUAL CHANGE" sheets, containing the required information. Replace affected pages or modify existing manual information as directed in the "MANUAL CHANGE" pages. Contact the nearest Hewlett-Packard Sales and Service Office if the change information is missing.

7-6. OLDER INSTRUMENTS

7-7. If your instrument's serial number prefix is lower than 2324A, perform the backdating that applies to your instruments serial prefix, as listed in *Table 7-1* below.

Table 7-1. Manual Backdating

If Instrument has Serial Prefix	Make the Following Changes to the Manual
2312A	1
2248A	1,2
2228A and 2204A	1,2,3

CHANGE 1 (2312A)

Page 6-15, Table 6-2, A2 Replaceable Parts:
Change A2 series number from 2324A to 2234A.
Change A2U10 from 1826-0909 to 1826-0627; IC OP AMP PRCN TO-99; 03285; AD542L.
Add A2Q1 and A2Q2: 1855-0402; TRANSISTOR-PFET; 28480; 2N5115.
Add under A2 MISCELLANEOUS PARTS: 0304-0060; Quantity 10; TERMINAL FEEDTHRU.

Page 6-21, Table 6-2, A5 Replaceable Parts:
Add under A5 MISCELLANEOUS PARTS: 0340-0060; Quantity 3; TERMINAL FEEDTHRU.
Change A5 series number from 2324A to 2204A.

Page 8-103, Figure 8-20, A2 Schematic Diagram:
In the ACTIVE COMPONENTS table:
Add A2Q1 and A2Q2, 1855-0402.
Change A2U10 from 1826-0909 to 1826-0627.
In the REFERENCE DESIGNATIONS table, change Q3-6 to Q1-6.
Change the series number on the A2 schematic from 2324A to 2234A.
Add Q1 and Q2 to the schematic as shown in *Figure 7-1*.

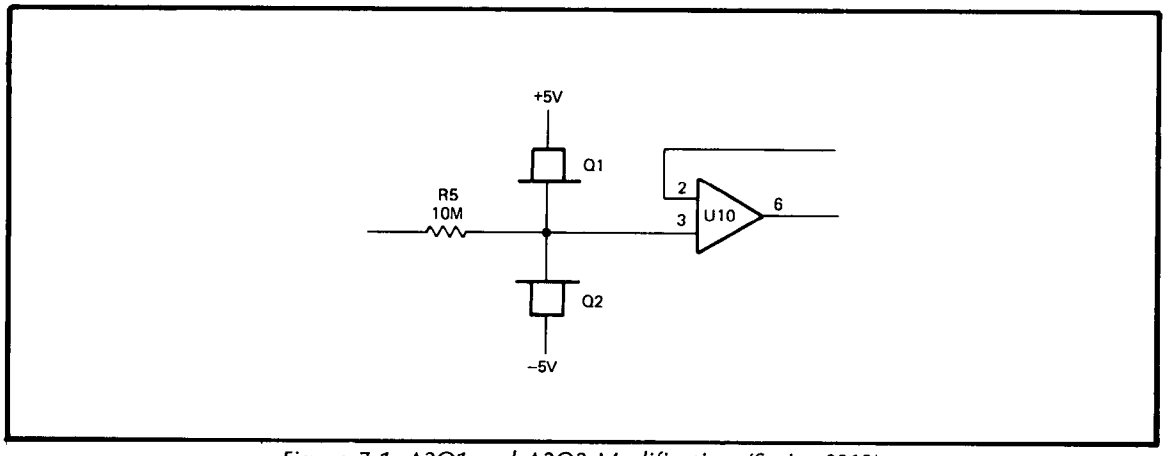


Figure 7-1. A2Q1 and A2Q2 Modification (Series 2312)

Page 8-109, Figure 8-23, A5 Schematic Diagram:
Change the series number on the A5 schematic from 2324A to 2204A.

NOTE

The cloverleafs were removed when a dry-film coating was applied to the circuit boards. This film ensures high immunity to humidity and a resulting high (>10^{12} ohms/sq. in.) impedance on the surface of the PCB.

CHANGE 2 (2248A)

Page 6-23, Table 6-2, A8 Replaceable Parts:
Change A8 series number from 2312A to 2248A.
Change A8CR6 from 1906-0229 DUAL 8 DIODE ARRAY to 1906-0202; DUAL 10 DIODE ARRAY; 1906-0202.

Page 8-111, Figure 8-24, A8 Schematic Diagram:
Change the series number on the A8 schematic from 2312A to 2248A.
Change A8CR6 in the ACTIVE COMPONENTS table to 1906-0202.
Change the A8 schematic diagram as shown in *Figure 7-2.*

NOTE

A change in vendors necessitated the change in diode arrays. The 1906-0202 has a different pin-out from the 1906-0229. Because of this, a revision was also made on the board blank for the A8 assembly. If the revision of your board is "A", then the 1906-0202 is the diode array to order as replacement. Revision "B" boards use the 1906-0229 diode array.

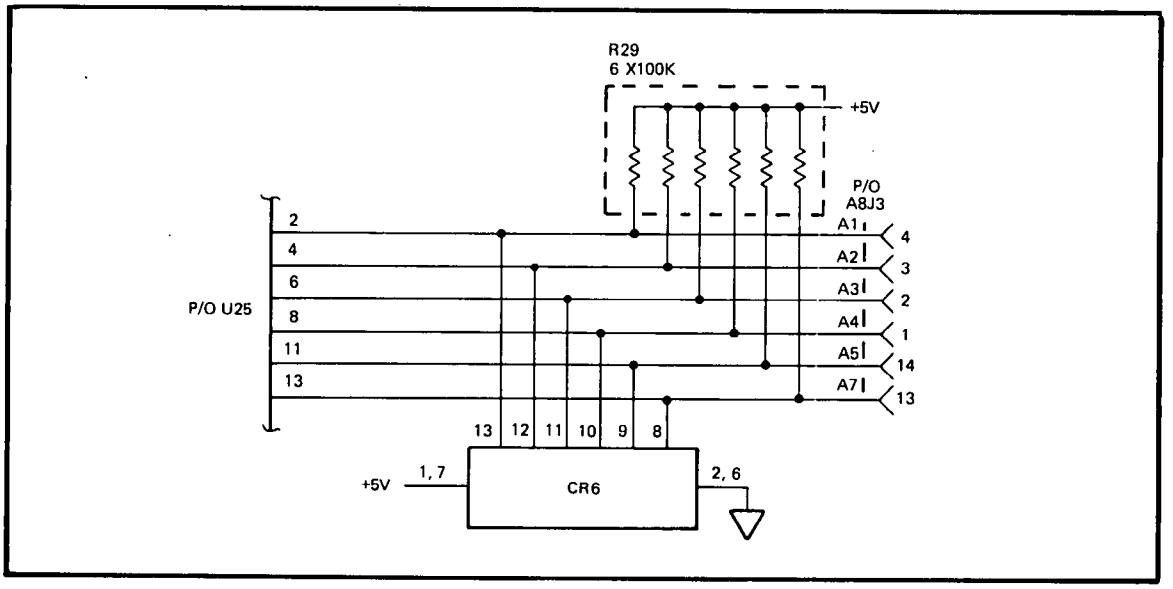


Figure 7-2. A8CR6 Modification (Series 2248A)

CHANGE 3
2228A ONLY

Page 6-23, Table 6-2, A8 Replaceable Parts:
Change A8 series number from 2248A to 2228A.
Change A8U23 from 1818-3161 to 05005-80006.

Page 8-111, Figure 8-24, A8 Schematic Diagram:
Change series number on the A8 schematic from 2248A to 2228A.
Change A8U23 in the ACTIVE COMPONENTS table to 05005-80006.

2204A ONLY

Page 6-23, Table 6-2, Replaceable Parts:
Change A8 series number from 2248A to 2204A.
Change A8U23 from 1818-3161 to 05005-80005.

Page 8-111, Figure 8-24, A8 Schematic Diagram:
Change series number on the A8 schematic from 2248A to 2204A.
Change A8U23 in the ACTIVE COMPONENTS table to 05005-80005.

NOTE

These changes were made to correct programming "bugs" in the EPROM. If a repalcement is to be made, 1818-3161 is now the preferred part.

SECTION VIII
SERVICE

8-1. INTRODUCTION

8-2. This section contains the information needed to service the HP Model 5005B. The information includes theory of operation, recommended test equipment, schematic diagram notes, safety considerations, assembly/disassembly procedures, troubleshooting information, and block and schematic diagrams. This section also includes a cross-reference table, *Table 8-1*, to aid the correlation of assembly reference designations with their HP part numbers.

8-3. THEORY OF OPERATION

8-4. The theory of operation is presented in three stages:

- General Instrument Description. These paragraphs present an overview of the operation and capability of the 5005B. This discussion references the Simplified Block Diagram in *Figure 8-9*.
- Block Diagram Description. These paragraphs describe the various Measurement Techniques and all Function Modes, and reference the Detailed Block Diagram in *Figure 8-18*.
- Detailed Circuit Theory. These paragraphs, arranged by assembly order, describe the individual circuits at the component level and reference the individual assembly schematic diagrams.

8-5. The schematic diagrams for the assemblies are located at the end of this section. They are arranged in numerical order according to the assembly number (i.e., A1, A2, A3, etc.) in *Figures 8-19* through *8-24*.

8-6. TROUBLESHOOTING

8-7. Troubleshooting for the 5005B is presented through a series of troubleshooting procedures. Many of the procedures utilize the built-in Diagnostics, designed to exercise and verify critical circuits using signature analysis, signal tracing, and conventional measurements. These procedures can efficiently isolate malfunctions to component level for diagnosis. Troubleshooting is keyed to the Overall Troubleshooting Flowchart in *Figure 8-12*.

8-8. RECOMMENDED TEST EQUIPMENT

8-9. Test equipment and test equipment accessories required to maintain the 5005B are listed in *Table 1-2*. Equipment other than that listed may be used if it meets the listed critical specifications. The following paragraphs describe additional equipment whose use is optional, but can prove very helpful during troubleshooting.

8-10. HP 545A Logic Probe, HP 546A Logic Pulser, and HP 547A Current Tracer

8-11. The Logic Probe, Logic Pulser, and Current Tracer are self-contained troubleshooting instruments designed to stimulate and measure digital activity in logic circuits. When bad signatures on a Signature Analyzer indicate printed circuit board opens or shorts, these instruments are very effective in isolating the specific point.

8-12. The Logic Probe is self-contained, easy-to-use tool for examining logic nodes. Continuity, signal flow, bus device, address decoder, clock, and switch activity of the 5005B may be verified. The circuit's operating characteristics while in defined diagnostic loops may be examined.

8-13. The Logic Pulser forces overriding pulses into nodes. It can be programmed to output single pulses, pulse streams, or bursts. The pulser can be used to force ICs to enable or clock. When used with the Logic Probe, logic circuit inputs can be pulsed while their outputs are monitored with the probe. By this means, correct signal propagation through logic elements can be verified.

8-14. The Current Tracer can be used to monitor current activity on a logic node or power bus, and can tell approximately how much pulse current is present and what path it takes. When a Logic Pulser is used to inject current into a nonactive (no pulse activity) node, the impedance and the nature of possible stuck nodes (e.g., output, hard short) can be estimated. Then the actual low impedance point can be found by tracing the path of the current from the Logic Pulser to the location where the current either goes to a short or enters a component.

8-15. SCHEMATIC DIAGRAM SYMBOLS AND REFERENCE DESIGNATORS

8-16. *Figure 8-1* shows the symbols used on the schematic diagrams. At the bottom of *Figure 8-1*, the system for reference designators, assemblies, and subassemblies is shown.

8-17. ASSEMBLY DESIGNATIONS

8-18. Assemblies such as printed circuit boards are assigned numbers in sequence, A1, A2, etc., as shown in *Table 8-1*. As shown in *Figure 8-1*, subassemblies within an assembly are given a subordinate A number. For example, rectifier subassembly A1, has the complete designator A25A1. For individual components, the complete designator is determined by adding the assembly number and subassembly number, if any. For example, CR1 on the rectifier assembly is designated A25A1CR1.

Table 8-1. Assembly Identification

ASSEMBLY	DESCRIPTION	HP PART NUMBER
A1	Main Assembly	05005-60011
A2	DVM Assembly	05005-60002
A3	Microprocessor and Display Drive Assembly	05005-60012
A4	Display and Keyboard Assembly	05005-60009
A5	Data Probe Assembly	05005-60010
A6	Timing Pod Assembly	05005-60013
A7	Line Module Assembly	0960-0444
A8	HP-IB Assembly	05005-60007
A9	HP-IB Interface Assembly	05005-60010

8-19. Identification Markings on Printed Circuit Boards

8-20. HP printed circuit boards (see *Figure 8-1*) have four verification numbers: an assembly part number, a series number, a revision letter, and a production code. The assembly part number has 10 digits (such as 05359-60021) and is the primary identification. All assemblies with the same part number are interchangeable. When a production change is made on an assembly that makes it incompatible with previous assemblies, a change in part number is required. The series number (such as 1748) is used to document minor electrical changes. As changes are made, the series number is incremented. When replacement boards are ordered, you may receive a replacement with a different series number. If there is a difference between the series number marked on the board and the schematic in this manual, a minor electrical difference exists. If the number on the printed circuit board is lower than that on the schematic, refer to Section VII for backdating information. If it is higher, refer to the yellow loose-leaf manual sheets for this

SYMBOLS

DANGEROUS VOLTAGE, EXCEEDS 1000 VOLTS

FRONT PANEL LABEL

REAR PANEL LABEL

INTERIOR AND PC BOARDS LABEL

WIPER MOVES TOWARD "CW" WHEN CONTROL IS ROTATED CLOCKWISE

OR PROTECTIVE CONDUCTOR TERMINAL

CIRCUIT COMMON

IDENTIFIED COMMON

OR CHASSIS TERMINAL

KNOB CONTROL

SCREWDRIVER ADJUST

MAIN SIGNAL PATH

FEEDBACK PATH

OR OR TEST POINT

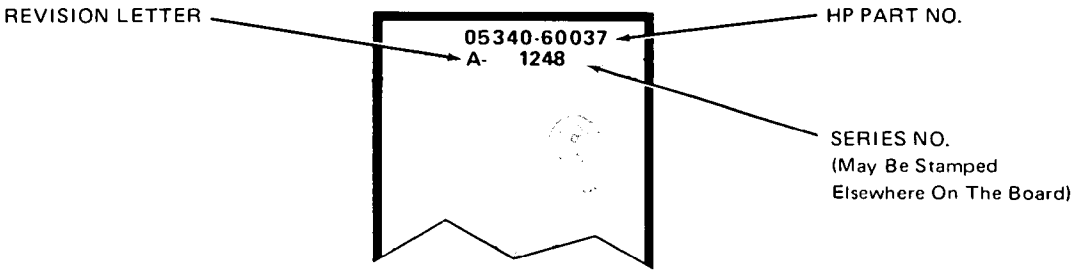
INSTRUCTION MANUAL REFERENCE

ALTERNATING CURRENT

DIRECT CURRENT

ALTERNATING OR DIRECT CURRENT

PRINTED CIRCUIT BOARD IDENTIFICATION



REFERENCE DESIGNATIONS

REFERENCE DESIGNATIONS WITHIN ASSEMBLIES ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION. JACKS ARE THE STATIONARY CONNECTORS AND PLUGS ARE THE MORE MOVEABLE OF TWO CONNECTORS.

ASSEMBLY	ABBREVIATION	COMPLETE DESCRIPTION
A25	C1	A25C1
A25A1	CR1	A25A1CR1
NO PREFIX	J3	J3

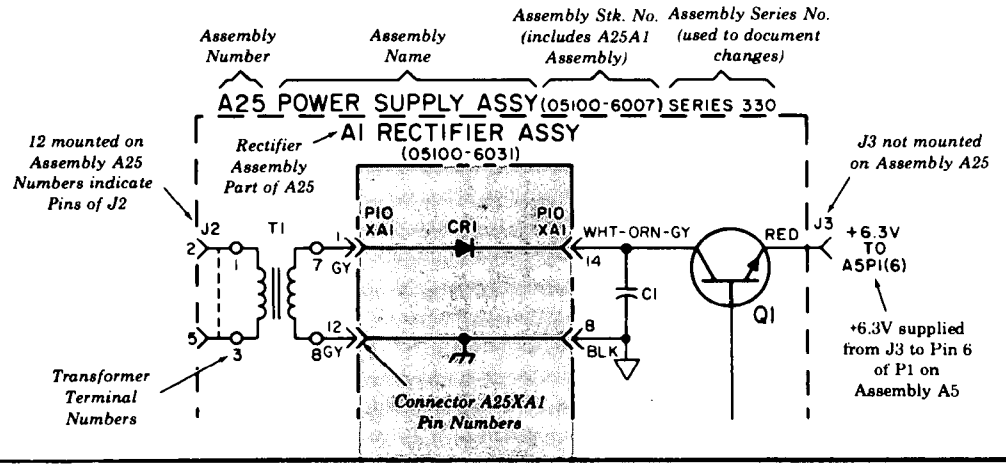


Figure 8-1. Schematic Diagrams Notes

manual. If the manual change sheets are missing, contact your local HP Sales and Service Office. See the listing on the back cover of this manual.

8-21. Revision letters (A, B, etc.) denote changes in printed circuit layout. For example, if a capacitor type is changed (electrical value may remain the same) and requires different spacing for its leads, the printed circuit board layout is changed and the revision letter is incremented to the next letter. When a revision letter changes, the series number is also usually changed. The production code is the four-digit, seven-segment number used for production purposes.

8-22. SAFETY CONSIDERATIONS

8-23. Although the 5005B has been designed in accordance with international standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the 5005B in safe operating condition. Service and adjustments should be performed only by qualified service personnel.

WARNING

ANY INTERRUPTION OF THE PROTECTIVE (GROUNDING) CONDUCTOR (INSIDE OR OUTSIDE THE 5005B) OR DISCONNECTION OF THE PROTECTIVE EARTH TERMINAL IS LIKELY TO MAKE THE 5005B DANGEROUS.

8-24. Any adjustment, maintenance, and repair of the opened 5005B under voltage should be avoided as much as possible and, when inevitable, should be carried out only by skilled personnel who are aware of the hazard involved. Capacitors inside the 5005B may still be charged even if the 5005B has been disconnected from its source of power.

8-25. Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short circuiting of fuseholders must be avoided. Whenever it is likely that this protection has been impaired, the 5005B must be made inoperative and be secured against any unintended operation.

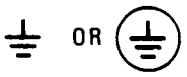
WARNING

THE SERVICE INFORMATION IS OFTEN USED WITH POWER SUPPLIED AND PROTECTIVE COVERS REMOVED FROM THE 5005B. ENERGY AVAILABLE AT MANY POINTS MAY, IF CONTACTED, RESULT IN PERSONAL INJURY.

8-26. Safety Symbols

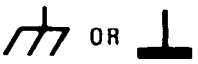
8-27. The following safety symbols are used on the instrument front panel, printed circuit boards, and in the manuals:

Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual to protect against damage to the instrument.



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with the symbol must be connected to ground in the manner described in the installation (operating) manual, before operating the equipment.



Frame and chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current.

Direct current.

Alternating or direct current.

The WARNING signal denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

8-28. SERVICE AIDS

8-29. *Pozidriv Screwdrivers.* Many screws in the 5005B appear to be Phillips type, but are not. To avoid damage to the screw slots, Pozidriv screwdrivers should be used.

8-30. *Service Aids on Printed Circuit Boards.* The servicing aids on the printed circuit boards include test points, reference designators, adjustment callouts, and assembly stock numbers.

8-31. *Diagnostic Routines.* The 5005B provides a selection of user designated self-diagnostic routines, which are permanently stored in ROM. These utilize interactive instrument testing with both conventional measurement techniques and digital Signature Analysis. The technician should have an understanding of the concepts of Signature Analysis as an in-circuit trouble-shooting technique. Hewlett-Packard makes available a variety of Application Notes on the

concepts and useage of Signature Analysis. It may be helpful to contact the nearest Hewlett-Packard Sales and Service Office (offices are listed at the back of this manual) and request a copy of the Signature Analysis publications index:

AN INDEX TO SIGNATURE ANALYSIS PUBLICATIONS, Application Note 222-0.

8-32. LOGIC SYMBOLS

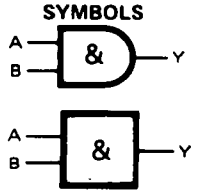
8-33. Logic symbols used in this manual conform to the American National Standard ANSI Y32.14-1973 (IEEE Std. 91-1973). This standard supersedes MIL-STD-806B. In the following paragraphs logic symbols are described. For further descriptions refer to HP Logic Symbology Manual, Part Number 5951-6116.

8-34. Logic Concepts

8-35. The binary numbers 1 and Ø are used in pure logic where 1 represents true, yes , or active and Ø represents false, no, or inactive. These terms should not be confused with the physical quantity (e.g., voltage) that may be used to implement the logic, nor should the term "active" be confused with a level that turns a device on or off. A truth table for a relationship in logic shows (implicitly or explicitly) all the combinations of true and false input conditions and the resultant (output). There are only two basic logic relationships, AND and OR. The following illustrations assume two inputs (A and B), but these can be generalized to apply to more than two inputs.

AND

EQUIVALENT SYMBOLS



TRUTH TABLE

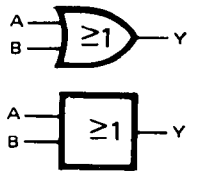
A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

Y is true if and only if A is true and B is true (or more generally, if all inputs are true).

Y = 1 if and only if A = 1 and B = 1.
Y = A · B

OR

EQUIVALENT SYMBOLS



TRUTH TABLE

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

Y is true if and only if A is true or B is true (or more generally, if one or more input(s) is (are) true).

Y = 1 if and only if A = 1 or B = 1.
Y = A + B

8-36. Negation

8-37. In logic symbology, the presence of the negation indication symbol O provides for the representation of the logic function inputs and outputs in terms *independent* of their physical values; the Ø-state of the input and output being the 1-state of the symbol referred to by the symbol description.

EXAMPLE 1

TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

Says that Z is not true if A is true and B is true or that Z is true if A and B are not both true. $\overline{Z} = AB$ or $Z = \overline{A} + \overline{B}$. This is frequently referred to as NAND (for NOT AND).

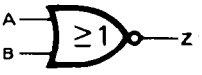
EXAMPLE 2

TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

Says that Z is true if A is not true or if B is not true. $Z = \overline{A} + \overline{B}$. Note that this truth table is identical to that of Example 1. This logic equation is merely a DeMorgan's transformation of the equations in Example 1. The symbols are equivalent.

EXAMPLE 3



TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

$\overline{Z} = A + B$ or $Z = \overline{AB}$.

EXAMPLE 4

TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

$Z = \overline{A} \cdot \overline{B}$, also share common truth table and and are equivalent transformations of each other. The NOT OR form (Example 3) is frequently referred to as NOR.

NOTE

In this manual the logic negation symbol is NOT used.

8-38. Logic Implementation and Polarity Indication

8-39. Devices that can perform the basic logic functions, AND and OR, are called gates . Any device that can perform one of these functions can also be used to perform the other if the relationship of the input and output voltage levels to the logic variables 1 and Ø is redefined suitably.

8-40. In decribing the operation of electronic logic devices, the symbol H is used to represent a "high level", which is a voltage within the more-positive (less-negative) of the two ranges of voltages used to represent the binary variable. L is used to represent a "low level", which is a voltage within the less-positive (more-negative) range.

8-41. A function table for a device shows (implicitly or explicitly) all the combinations of input conditions and the resulting output conditions.

8-42. In graphic symbols, inputs or outputs that are active when at the high level are shown without polarity indication. The polarity indicator symbol ◺ denotes that the active (one) state of an input or output *with respect to the symbol to which it is attached* is low level.

NOTE

The polarity indicator symbol ◺ is used in this manual.

EXAMPLE 5

DEVICE #1
FUNCTION TABLE

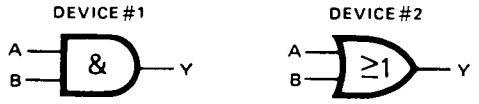
A	B	Y
H	H	H
H	L	L
L	H	L
L	L	L

DEVICE #2
FUNCTION TABLE

A	B	Y
H	H	H
H	L	H
L	H	H
L	L	L

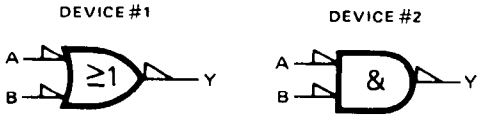
Assume two devices having the following function tables.

POSITIVE LOGIC



By assigning the relationships H = 1, L = Ø at both input and output, Device #1 can perform the AND function and Device #2 can perform the OR function. Such a consistent assignment is referred to as positive logic.

NEGATIVE LOGIC



Alternatively, by assigning the relationship H = Ø; L = 1 at both input and output, Device #1 can perform the OR function and Device #2 can perform the AND function. Such a consistent assignment is referred to as negative logic. The corresponding logic symbols would be:

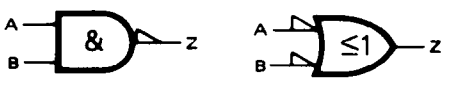
8-43. MIXED LOGIC. The use of the polarity indicator symbol on some inputs (◺) automatically invokes a mixed-logic convention. This is, positive logic is used at the inputs and outputs that have polarity indicators, negative logic is used at the inputs and outputs that have polarity indicator.

EXAMPLE 6

EXAMPLE 6
FUNCTION TABLE

A	B	Z
H	H	L
H	L	H
L	H	H
L	L	H

This may be shown either of two ways:



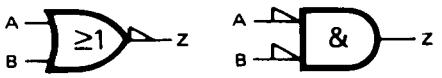
Note the equivalence of these symbols to Examples 1 and 2 and the fact that the function table is a positive-logic translation (H = 1, L = Ø) of the NAND truth table, and also note that the function table is the negative-logic translation (H = Ø, L = 1) of the NOR truth table, given in Example 3.

EXAMPLE 7

EXAMPLE 7
FUNCTION TABLE

A	B	Z
H	H	L
H	L	L
L	H	L
L	L	H

This may be shown either of two ways:



Note the equivalence of these symbols to Examples 3 and 4 and the fact that the function table is a positive-logic translation (H = 1, L = Ø) of the NOR truth table, and also note that the function table is the negative-logic translation (H = Ø, L = 1) of the NAND truth table, given in Example 1.

8-44. It should be noted that one can easily convert from the symbology of positive-logic merely by substituting a polarity indicator (◺) for each negative indicator (O) while leaving the distinctive shapes alone. To convert from the symbology of negative-logic, a polarity indicator (◺) is substituted for each negation indicator (O) and the OR shape is substituted for the AND shape or vice versa.

8-45. It was shown that any device that can perform OR logic can also perform AND logic and vice versa. DeMorgan's transformation is illustrated in Examples 1 through 7. The rules of the transformation are:

1. At each input or output having a negation (O) or polarity (◺) indicator, delete the indicator.
2. At each input and output not having an indicator, add a negation (O) or polarity (◺) indicator.
3. Substitute the AND symbol (⊐) for the OR symbol (⊃) or vice versa. These steps do not alter the assumed convention; positive-logic stays positive, negative-logic stays negative, and mixed-logic stays mixed.

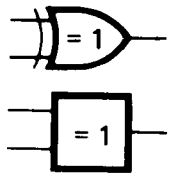
8-46. The choice of symbol may be influenced by these considerations: (1) The operation being performed may best be understood as AND or OR. (2) In a function more complex than a basic gate, the inputs will ususally be considered as inherently active high or active low (e.g.,the J and K inputs of a J-K flip-flop are active high and active low, respectively). (3) In a chain of logic, understanding and the writing of logic equations are often facilitated if active low or negated outputs feed into active low or negated inputs.

8-47. Other Symbols

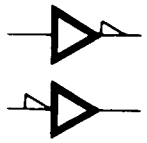
8-48. Additional symbols are required to depict complex logic diagrams, as follows:

Dynamic input activated by transition from a low level to a high level. The opposite transition has no effect at the output.

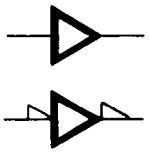
Dynamic input activated by transition from a high level to a low level. The opposite transition has no efect at the output.



Exclusive OR function. The output will assume its indicated active level if and only if one and only one of the inputs assumes its indicated active level.

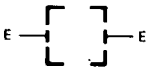


Inverting function. The output is low if the input is high and it is high if the input is low. The two symbols shown are equivalent.

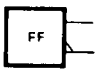


Noninverting function. The output is high if the input is high and it is low if the input is low. The two symbols shown are equivalent.

OUTPUT DELAY. The output signal is effective when the input signal returns to its opposite state.



EXTENDER. Indicates when a logic function increases (extends) the number of inputs to another logic function.



FLIP-FLOP. A binary sequential element with two stable states: a set (1) state and a reset (Ø) state. Outputs are shown in the 1-state when the flip-flop is set. In the reset state the outputs will be opposite to the set state.

RESET. A 1 input will reset the flip-flop. A return to Ø will cause no further effect.

SET. A 1 input will set the flip-flop. A return to Ø will cause no further effect.

TOGGLE. A 1 input will cause the flip-flop to change state. A return to Ø will cause no further action.

J INPUT. Similar to the S input except if both J and K (see below) are at 1, the flip-flop changes.

K INPUT. Similar to the R input (see Reset).

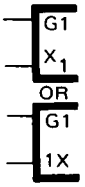
D INPUT (Data). Always dependent on another input (usually C). When the C and D inputs are at 1, the flip-flop will be set. When the C is 1 and the D is Ø, the flip-flop will reset.

ADDRESS. Address symbol has multiplexing relationship at inputs and demultiplexing relationship at outputs.

8-49. Dependency Notation "C" "G" "V" "F"

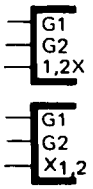
8-50. Dependency Notation is a way to simplify symbols for complex IC elements by defining the existence of an AND relationship between inputs, or by the AND conditioning of an output by an input without actually showing all the elements and interconnections involved. The following examples use the letter "C" for control and "G" for gate. The dependent input is labeled with a number that is either prefixed (e.g., 1X) or subscripted (e.g., X_1). They both mean the same thing. The letter "V" is used to indicate an OR relationship between inputs and outputs with this letter (V). The letter "F" indicates a connect-disconnect relationship. If the "F" (free dependency) inputs and outputs are active (1) the other usual normal conditions apply. If one or more of the "F" inputs are inactive (Ø), the related "F" output is disconnected from its normal output condition (it floats).

The input that controls or gates other inputs is labeled with a "C" or a "G", followed by an identifying number. The controlled or gated input or output is labeled with the same number. In this example, "1" is controlled by "G1".



When the controlled or gated input or output already has a functional label (X is used here), that label will be prefixed or subscripted by the identifying number.

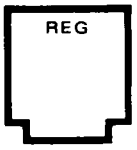
If a particular device has only one gating or control input then the identifying number may be eliminated and the relationship shown with a subscript.



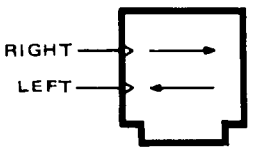
If the input or output is affected by more than one gate or control input, then the identifying numbers of each gate or control input will appear in the prefix or subscript, separated by commas. In this example "X" is controlled by "G1" and "G2".

8-51. Control Blocks

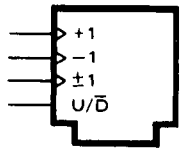
8-52. A class of symbols for complex logic are called control blocks. Control blocks are used to show where common control signals are applied to a group of functionally separate units. Examples of types of control blocks follow:



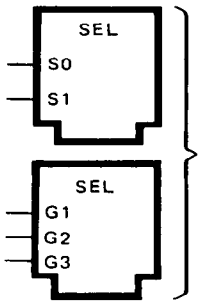
Register control block. This symbol is used with an associated array of flip-flop symbols to provide a point of placement for common function lines, such as a common clear.



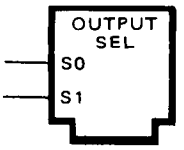
Shift register control block. These symbols are used with any array of flip-flop symbols to form a shift register. An active transition at the inputs causes left or right shifting as indicated.



Counter control block. The symbol is used with an array of flip-flops or other circuits serving as a binary or decade counter. An active transition at the +1 or -1 input causes the counter to increment one count upward or downward, respectively. An active transistion at the ±1 input causes the counter to increment one count upward or downward depending on the input at an up/down control.



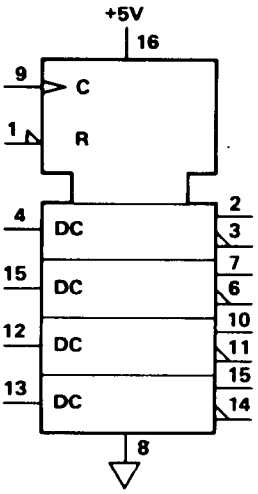
Selector control block. These symbols are used with an array of OR symbols to provide a point of placement for selection (S) or gating (G) lines. The selection lines enable the input designated Ø, 1, ...n of each OR function by means of a binary code where SØ is the least significant digit. If the 1 level of these lines is low, polarity indicators (◺) will be used. The gating lines have an AND relation with the respective input of each OR function: G1 with the inputs numbered 1, G2 with the inputs numbered 2, and so forth. If the enabling levels of these lines are low, polarity indicators (◺) will be used.



Output selector control block. This symbol is used with a block symbol having multiple outputs to form a decoder. The selection lines enable the output designated Ø, 1, ...n of each block by means of a binary code where SØ is the least significant digit. If the 1 level of these lines is low, polarity indicators (◺) will be used.

8-53. Complex Logic Devices

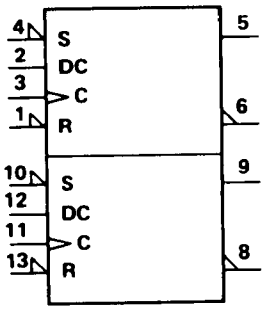
8-54. Logic elements can be combined to produce very complex devices that can perform more difficult functions. A control block symbol can be used to simplify understanding of many complex devices. Several examples of complex devices are given here. These examples are typical of the symbols used in schematic diagrams in this manual.



QUAD D-TYPE FLIP-FLOPS

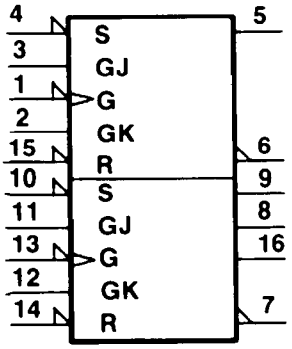
Data at the DC inputs is transferred to the outputs on the positive-going edge of the clock pulse (pin 9). A **LOW** signal at the reset (pin 1) will clear all FFs.

DUAL D-TYPE FLIP-FLOP

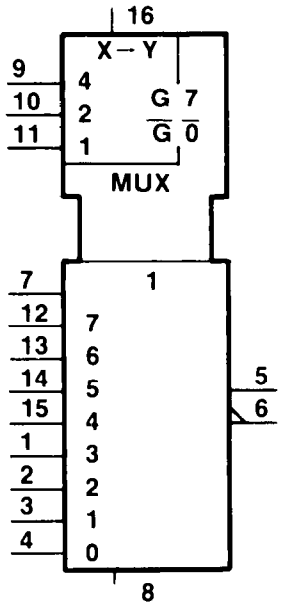


The dual D-type flip-flop consists of two independent D-type flip-flops. The information present at the data (D_C)input is transferred to the active-**HIGH** and active-**LOW** outputs on a low-to-high transition of the clock (C) input. The data input is then locked out and the outputs do not change again until the next **LOW**-to-**HIGH** transition of the clock input. The set (S) and reset (R) inputs override all other input conditions: when (S) is **LOW**, the active-HIGH output is forced **HIGH**; when reset (R) is **LOW**, the active-high output is forced **LOW**. Although normally the active-**LOW** output is the complement of the active-**HIGH** output, simultaneous **LOW** inputs at the set and reset will force both the active-**LOW** and active-**HIGH** outputs to go **HIGH** at the same time on some D-type flip-flops. This condition will exist only for the length of time that both set and reset inputs are held **LOW**. The flip-flop will return to some indeterminate state when both the set and reset inputs are returned to the **HIGH** state.

DUAL J-K FLIP-FLOPS WITH CLEAR AND PRESET

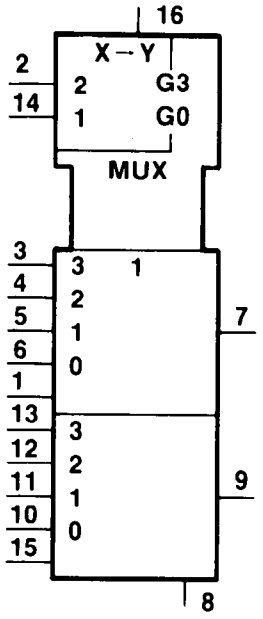


The dual J-K flip-flop consists of two independent J-K type flip-flops. The flip-flop response is determined by the states of GJ and GK inputs, at the instant that a **LOW**-going transition is applied to the G input. When GJ and GK are **LOW**, the outputs will not change state. When GJ is **LOW** and GK is **HIGH**, the Q output (pin 5 or 9) will go **LOW** (unless it is already **LOW**). When GJ is **HIGH** and GK is **LOW**, the Q output (pin 5 or 9) will go **HIGH** (unless it is already **HIGH**). When GJ and GK are both **HIGH**, the output will change state with each negative going edge transition at G. The S (set) and R (reset) inputs override all other input conditions: when S is **LOW**, Q is forced **HIGH**; when R is **LOW**, Q is forced **HIGH**. The $\overline{Q}$ output (pin 6 or 7) operates as the complement of the Q output (pin 5 or 9).



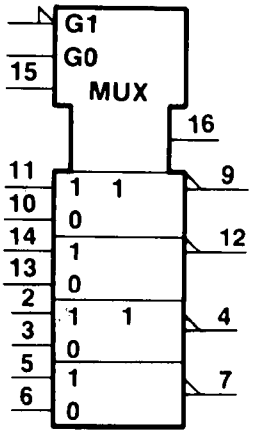
DATA SELECTOR/MULTIPLEXER

This data multiplexer selects one of eight line inputs, directing it and its complement to the output when enabled. Pins 11, 10, and 9 are the binary weighted "1", "2", and "4" select inputs, respectively. A **LOW** on the enable (pin 7) will direct the selected input line data to the output (pin 5). An inverted output of the selected input line data is provided at pin 6.



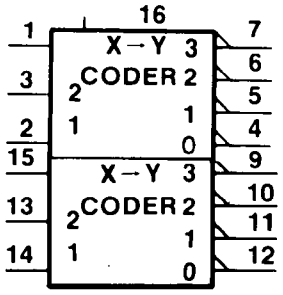
DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXERS

This dual four input multiplexer selects one of four line inputs directing it to the output when enabled. Pins 14 and 2 are the binary weighted "1" and "2" select inputs, respectively. A **LOW** on the enable (pin 1 or 15 or both) will direct the selected input line data to the respective output.



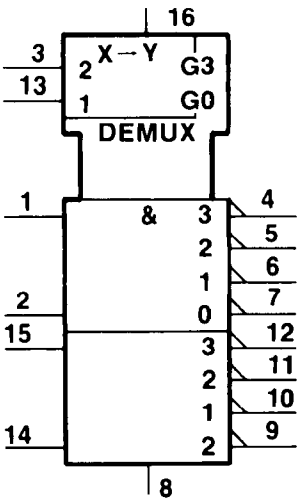
QUAD 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXERS

This quad two input multiplexer selects one of two word inputs directing it to the output when enabled. The level at G1/G0 (pin 1) selects the input line for all four selectors; a **HIGH** selects input "Ø", a **LOW** selects input "1". The selected inputs are inverted and directed to their respective outputs unless inhibit line (pin 15) is **HIGH**. When inhibit (pin 15) is **HIGH**, all outputs go **HIGH**.



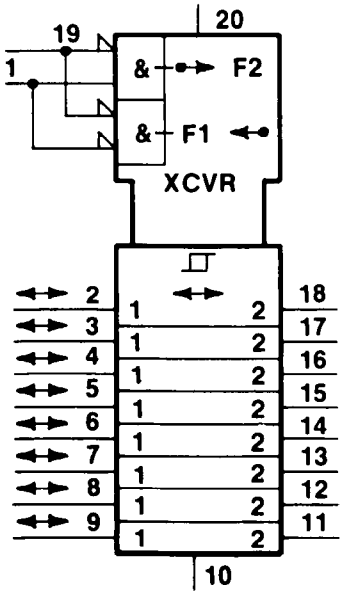
DUAL DECODER/DEMULTIPLEXERS

This device consists of two independent two-line to four-line decoders. Pins 2 (14) and 3 (13) are the binary weighted "1" and "2" select lines, respectively. The selected output is forced **LOW**, unless the inhibit (pin 1 or 15) is **HIGH**. When the inhibit is **HIGH**, all respective decoder outputs go **HIGH**.



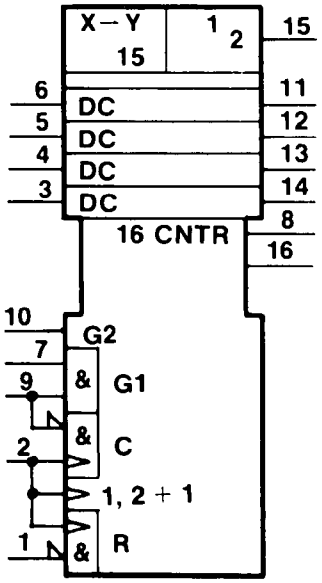
DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXERS

This device consists of two separate two-line to four-line decoders, with common select lines. Pins 13 and 3 are the binary weighted "1" and "2" select lines, respectively. The output selected is forced **LOW** on both decoder halves. All other outputs are **HIGH**.



OCTAL BUS TRANSCEIVERS WITH 3-STATE Outputs

This octal transceiver is an eight-line bidirectional bus transceiver with 3-State outputs. The direction of data transfer is determined by pin 1; a **HIGH** directs the data from the "1" bus to the "2" bus if enabled, a **LOW** directs the data from the "2" bus to the "1" bus if enabled. Pin 19 is the enable. When pin 19 is **LOW**, data transfer is enabled in the selected direction. When pin 19 is **HIGH**, data transfer is disabled and both output buses are set to the high impedance state.



SYNCHRONOUS DECADE COUNTER

This synchronous presettable decade counter has four master slave flip-flops that are triggered on the positive-going edge of the clock pulse (pin 2). A **LOW** at the load input (pin 9) disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels at the enable inputs (pin 7 and 10). The clear function (pin 1) is synchronous and a **LOW** level clear input sets all outputs **LOW** regardless of the levels of the clock, load or enable inputs. Both count enable inputs (pins 7 and 10) must be **HIGH** to count and the pin 10 input is fed forward to enable the carry output (pin 15).

8-55. REPAIR TECHNIQUES

8-56. Handling and Cleaning of the A2 DVM Assembly

8-57. The A2 DVM assembly is a high impedance printed circuit board. Areas of the printed circuit board are highly susceptible to contamination from dirt and oils when handled. It is recommended that the A2 DVM assembly be handled ONLY by the edges. Avoid contact with the printed circuit areas, **especially the area around K1, K2, U3, and U4**, with bare fingers. If the printed circuit board surface is contaminated, the DVM may operate in a nonlinear fashion. If this occurs, clean the assembly before attempting to replace components.

8-58. The A2 assembly should be cleaned whenever repairs are completed, or contamination is suspected. The following steps describe the recommended procedure for the repair and cleaning of a high impedance printed circuit board.

a. When replacing components, ALWAYS use a water soluble acid core solder (e.g., HP Part No. 8090-0736).

b. Hand wash the printed circuit board, using distilled water, powdered detergent, and a small nonmetallic brush with natural bristles. Rinse with distilled water, removing as much soap residue as possible.

CAUTION

Assembly mounted switches and potentiometers may be damaged by cleaning. Remove these types of components if mounted in sockets. Relubricate any of these components which are cycled through a cleaning procedure.

c. Next, auto wash using an automatic wash machine, or home type dishwasher. Add dishwasher detergent and cycle.

d. After washing, bake the assembly in a hot chamber or home oven for 24 hours, at 50°C (~150°F). This is to remove all remaining moisture.

e. After baking, and preferably while still warm, spray both sides of the assembly with a light coat of clean, clear plastic type protectant coating. This seals the assembly from moisture and humidity.

NOTE

High impedance printed circuit boards can also be cleaned with a high quality solvent or degreaser, such as FREON TF® (HP Part No. 8500-0232). Never use a cleaner that contains oils or that leaves a residue. Spray or brush lightly, then rinse with isopropyl alcohol, blow dry with compressed air, bake for 24 hours, and spray coat as described above. Note, however, that this type of cleaning will remove the protectant coating applied at the factory. Always recoat the assembly with a plastic type protective spray whenever a solvent or degreaser is used.

®"FREON" is a registered DuPont trademark.

8-59. Removal of Assembly Plastic Hinges

8-60. The A1, A2, A3, and A8 assemblies are connected together by interlocking black plastic hinges. Two hinges are mounted to each assembly, pressed into alignment slots, and secured with a small drop of super adhesive.

8-61. The hinges are not normally intended to be removed. Should one become cracked or broken, it can be removed and replaced. To remove, heat the damaged part with a heat gun (hair dryer), occasionally rocking back and forth, until it loosens. Pull the part straight off, away from the board edge. Place a drop of adhesive near the PC board slot, and quickly install the new part. Be sure to properly position the new hinge before mounting. The posts should always point to the left, while looking at the J1 60-pin connector edge of the assembly.

8-62. Disassembly and Reassembly

8-63. The following procedures are divided into two categories: Main Cabinet Disassembly and PC Board Removal. The Main Cabinet Disassembly procedures open the instrument and, utilizing the hinged PC board feature, allow serviceable access to all the assemblies within the HP 5005B, under normal power-up conditions. Following this, the PC Board Removal procedures describe how to disassemble and remove each of the individual assemblies from the instrument. Reassembly is essentially the reverse of the disassembly procedures.

8-64. The following tools are required for these procedures:

a. Large Pozidriv screwdriver.
b. Small Pozidriv screwdriver.
c. Small flat-bladed screwdriver.
d. Needle-nose pliers.

8-65. Before performing any of the following disassembly or reassembly procedures:

a. Set LINE switch to OFF.
b. Remove the line power cable from the rear panel power module.

WARNING

LINE VOLTAGE IS EXPOSED WITHIN THE 5005B EVEN WHEN THE LINE SWITCH IS SET TO OFF. REMOVAL OF THE POWER CORD IS NECESSARY TO FULLY UNPOWER THE 5005B.

8-66. MAIN CABINET DISASSEMBLY

a. REMOVAL OF THE TOP COVER. Remove the recessed Pozidriv screw at the rear of the handle. Slide the top cover to the rear 1/4 of an inch and lift off.

b. REMOVAL OF THE BOTTOM COVER. Turn the instrument upside-down and loosen the recessed Pozidriv screw loated in ther rear edge of the bottom cover. The screw does not come out of the cover; loosen it until the cover can be removed. Slide the bottom cover to the rear until it can be lifted off.

c. REMOVAL OF TOP STRUT. Remove the four recessed Pozidriv screws (two on each side), and lift straight up on the Top Strut.

d. REPOSITION THE FRONT PANEL ASSEMBLY. Release the clamp from the grey ribbon cable that connects the A8 HP-IB Microprocessor assembly to the Front Panel assembly. Remove the four recessed Pozidriv screws holding the Front Panel frame to the side struts of the main chassis. Carefully pull the Front Panel assembly away from the instrument, simultaneously pushing the Data Probe and Timing Pod cables through the front panel cable boots. (See *Figure 8-2.*)

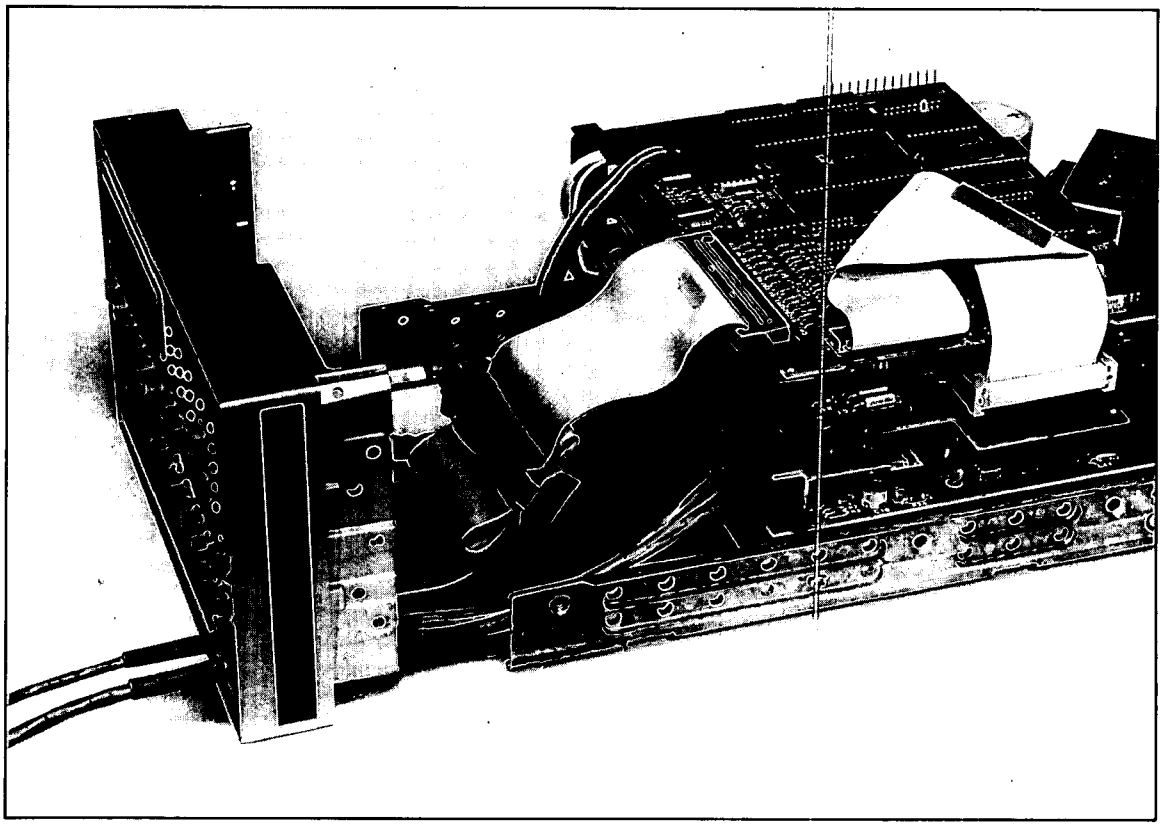


Figure 8-2. Reposition Front Panel

e. RAISING THE HINGED PC BOARDS. The top three circuit boards are hinged for ease of service. Do not remove them from the hinges unless necessary. There are two white plastic standoffs near the rear of each of the bottom three circuit boards. These standoffs have locks to hold the hinged boards in place during normal use.

WARNING

THE A2 DVM PRINTED CIRCUIT BOARD IS A HIGH IMPEDANCE PC BOARD. IT IS EXTREMELY SENSITIVE TO CONTAMINATION FROM DIRT AND OILS, APPLIED WHEN HANDLING WITH BARE HANDS. CONTAMINATION CAN CAUSE DRIFT, NONLINEARITY, OR IN-OPERATION. DO NOT HANDLE THE A2 DVM ASSEMBLY WITH BARE FINGERS, EXCEPT AT THE EDGES.

8-67. To release the standoffs, squeeze the protruding catch with a needle-nose pliers while lifting the corner of the circuit board. (See *Figure 8-3.*) After releasing both corners in this manner, the A8 board can be swung out of the way on its hinges.

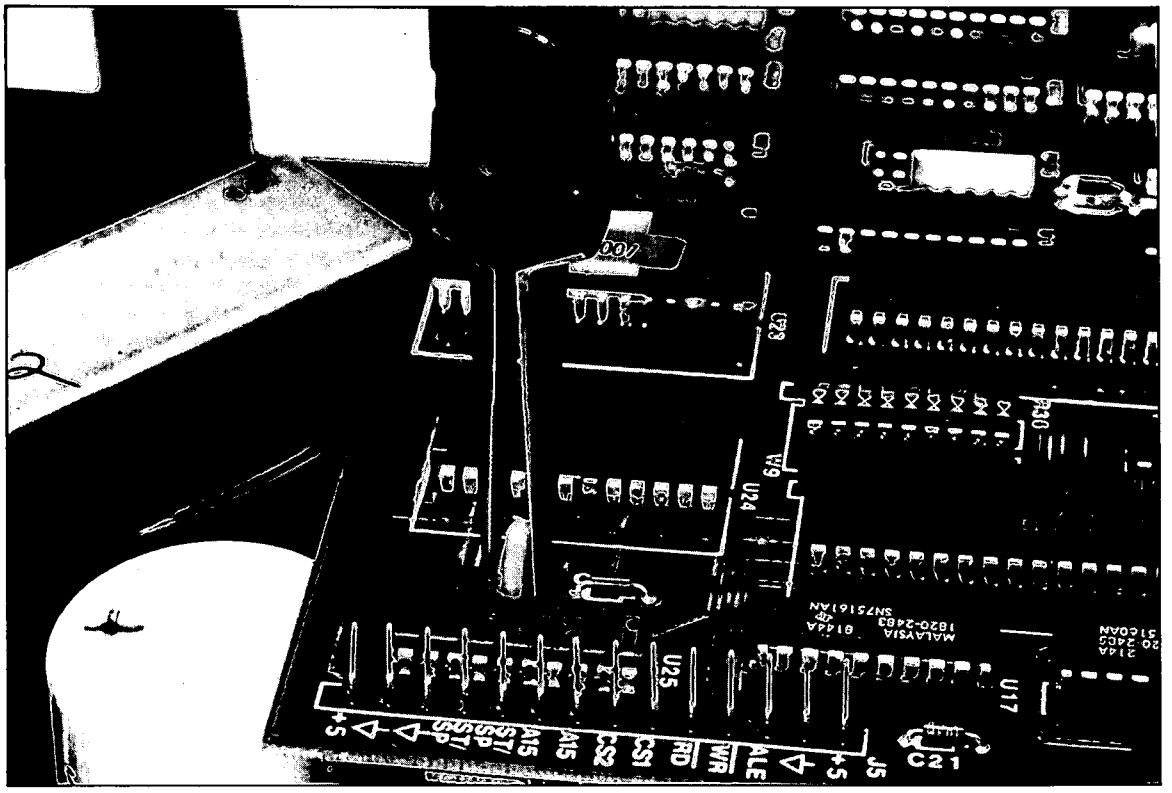


Figure 8-3. Locking Standoff Release

8-68. Using the above procedure, release the locks on the A3 standoffs, and raise the A3 Microprocessor assembly up on its hinge, about 90°. The A8 HP-IB assembly will continue traveling to a horizontal position. Release the locks on the A2 DVM assembly and raise it in a similar manner to the A3 assembly. At this time, the A8, A3, A2, and A1 assemblies are all accessible, and if power is applied, the instrument can be operated normally. See *Figure 8-4.*

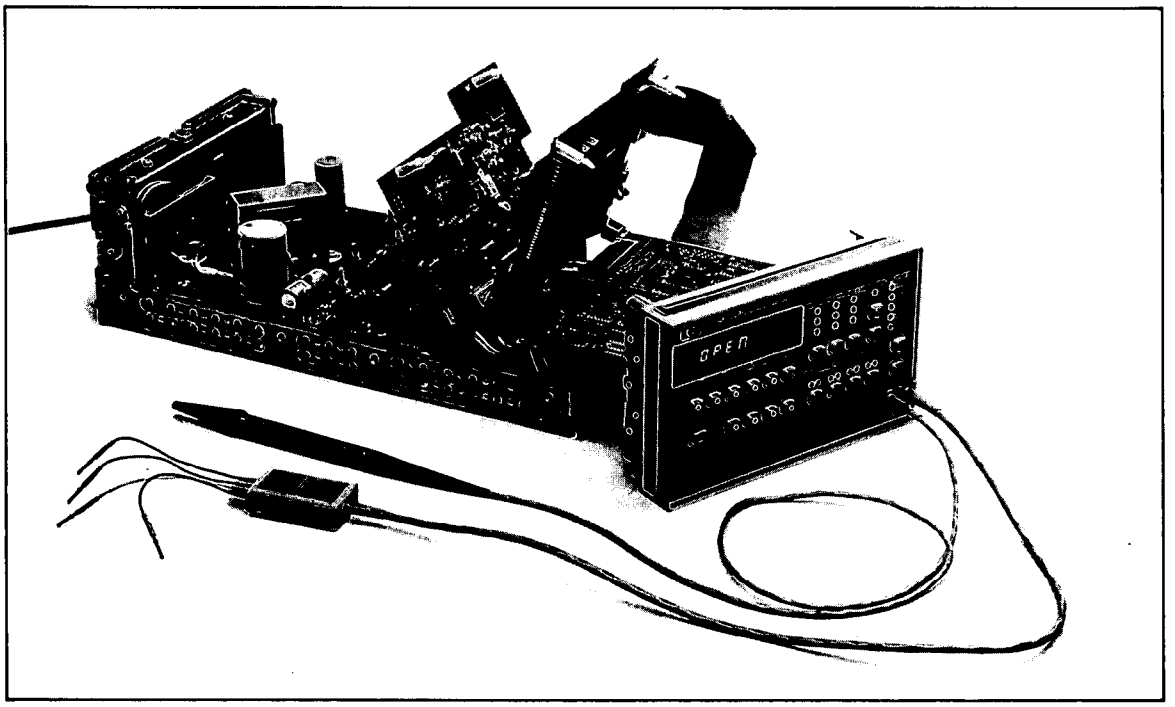


Figure 8-4. Open and Operating

8-69. PC BOARD REMOVAL

8-70. Before performing any of the following disassembly or reassembly procedures:

a. Set LINE switch to OFF.
b. Remove the line power cable from the rear panel power module.

8-71. To remove the individual printed circuit board assemblies, first perform steps a through e. in paragraph 8-66, then proceed as follows:

WARNING

LINE VOLTAGE IS EXPOSED WITHIN THE 5005B EVEN WHEN THE LINE SWITCH IS SET TO OFF. REMOVAL OF THE POWER CORD IS NECESSARY TO FULLY UNPOWER THE 5005B.

8-72. A4 Display Assembly Removal

8-73. Removal of the A4 Display Assembly first requires removal of the Front Panel from the front panel housing (see *Figure 8-5*). Disconnect the edge connector on the 50-line flat ribbon cable at the front side of the A8 HP-IB assembly. Slide the front panel assembly forward, carefully feeding the Data Probe and Timing Pod cables through the boots. Remove the trim strip at the top of the Front Panel using a small flat-bladed screwdriver. Remove the four recessed Pozidriv screw (two on the top, two on the bottom) holding the front subpanel to the front frame. Remove the frame from the front subpanel. At this point, the Data Probe and Timing Pod cable boots may be removed by sliding them to the right side of the front panel. The window is removed by sliding it to the left.

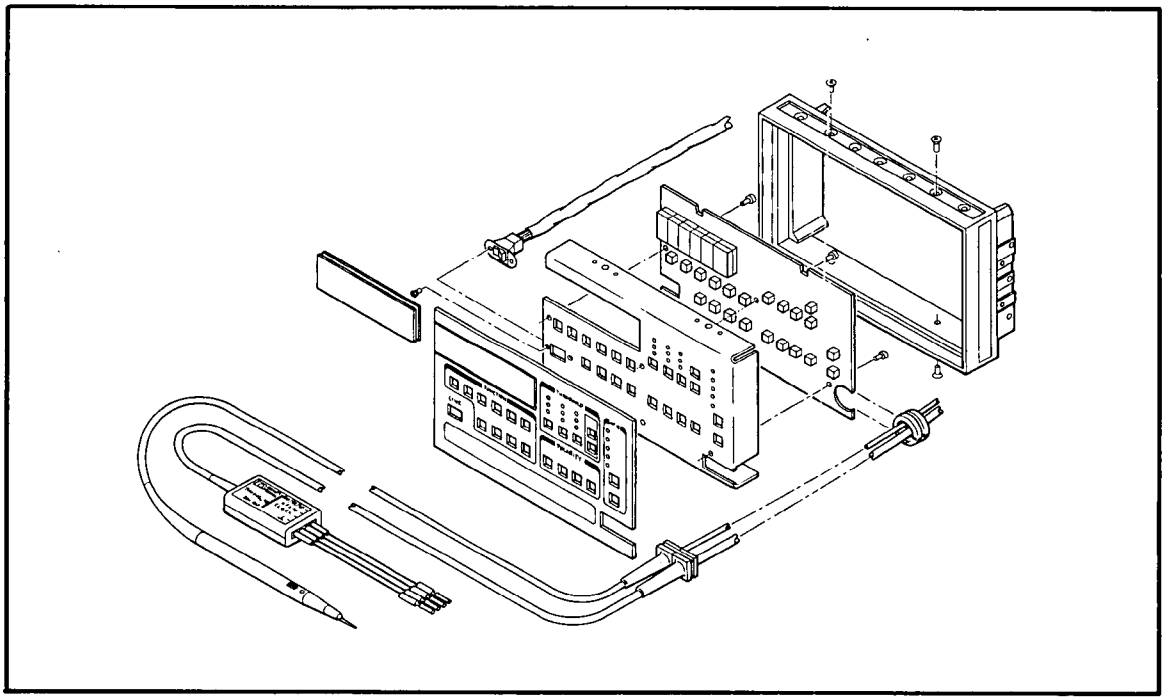


Figure 8-5. Removing A4 Display Assembly

8-74. The A4 Display assembly can be removed by removing six Pozidriv screws holding it to the subpanel. The Line Switch can only be removed by separating the Front Dress panel from the

subpanel. These are attached with double-sided tape. Separation of these panels should be done only if absolutely necessary.

8-75. A7 Line Module/Rear Panel Disassembly

8-76. Rear Panel/Line Module removal. Remove the four recessed Pozidriv screws holding the Rear Panel assembly to the chassis side frames. Disconnect the 24-pin connector from the A9 HP-IB Interface assembly and disconnect all the push-on wires from the A7 Line Module (see *Figure 8-19* for proper reconnection of the wires to the A7 assembly). The Rear Panel can be separated from the rear frame by removing the four Pozidriv screws holding them together. The A9 HP-IB Interface assembly is held in place by two 7mm hex studs, which can be removed with a 9/32" nut driver, should no metric tools be available.

8-77. A6 Timing Pod Disassembly

8-78. The Timing Pod halves are secured together by four locking retainers, two located on either side of the pod. To disassemble the pod, insert the tip of a small flat-bladed screwdriver, pressing in on the retainer, while gently separating the pod halves. Note the positions of the wire colors as a reminder for reassembly; green = ST/SP/START, red = QUAL/STOP, yellow = CLOCK, and black ⊥. The metal shield may be removed by removing the two retaining screws. Note the insulator on the inside of the shield. When reassembling, insure the shield is folded such that the insulator is replaced between the PC board and the shield. See *Figure 8-6*.

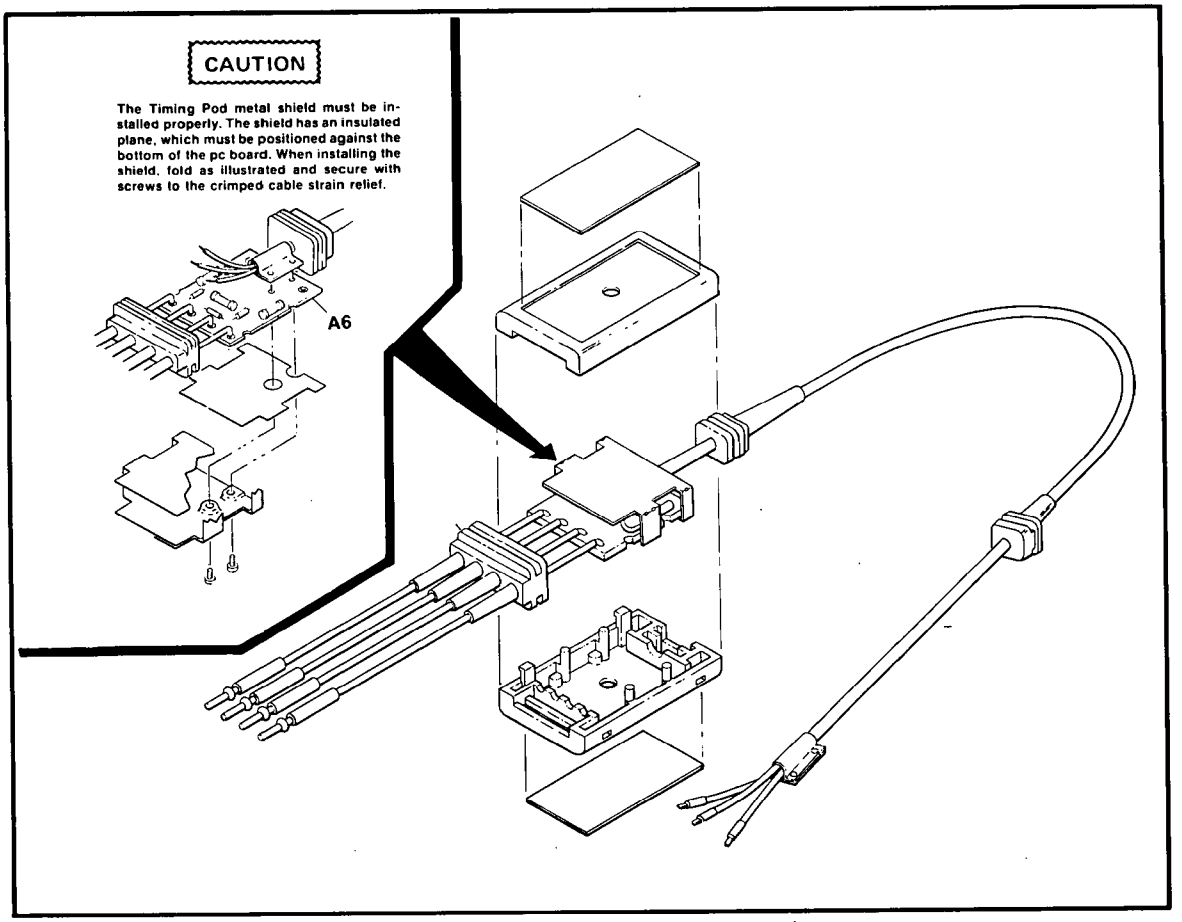


Figure 8-6. Disassembled Timing Pod

8-79. A5 Data Probe Disassembly

8-80. To disassemble the Data Probe, unscrew the Data Probe tip and pull off the red window. Slide the bottom probe body half off first, (this is the probe body half without the ground pin). Lift the top probe body off, being careful not to bend the ground pin or the switch, which both protrude slightly through the probe body half. The A5 Data Probe Assembly printed circuit board can be removed from the cable boot by firmly grasping the boot, while gently flexing the the PC board, rocking it side to side, until it clears the stops on the boot. See *Figure 8-7.*

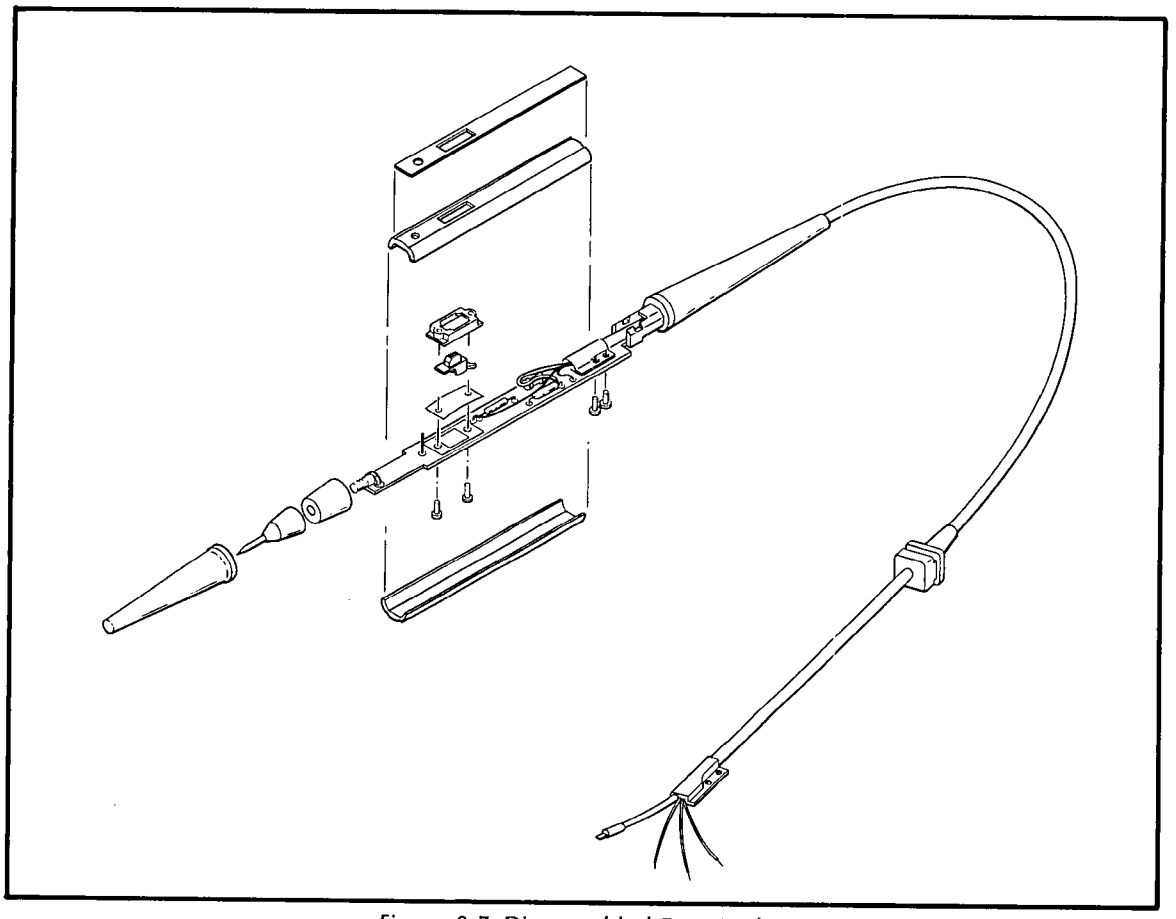


Figure 8-7. Disassembled Data Probe

8-81. A8 HP-IB Assembly Removal

8-82. To remove the A8 assembly, disconnect the 50-line ribbon cable, the 24-line HP-IB cable, and the four-line power cable from the front edge of the board. Release the standoffs as described in paragraph 8-66(e) and raise the A8 assembly on its hinges. Disconnect the 34-line ribbon cable from the right side of the A3 Microprocessor assembly. Remove the A8 assembly by sliding it to the right. See *Figure 8-8.*

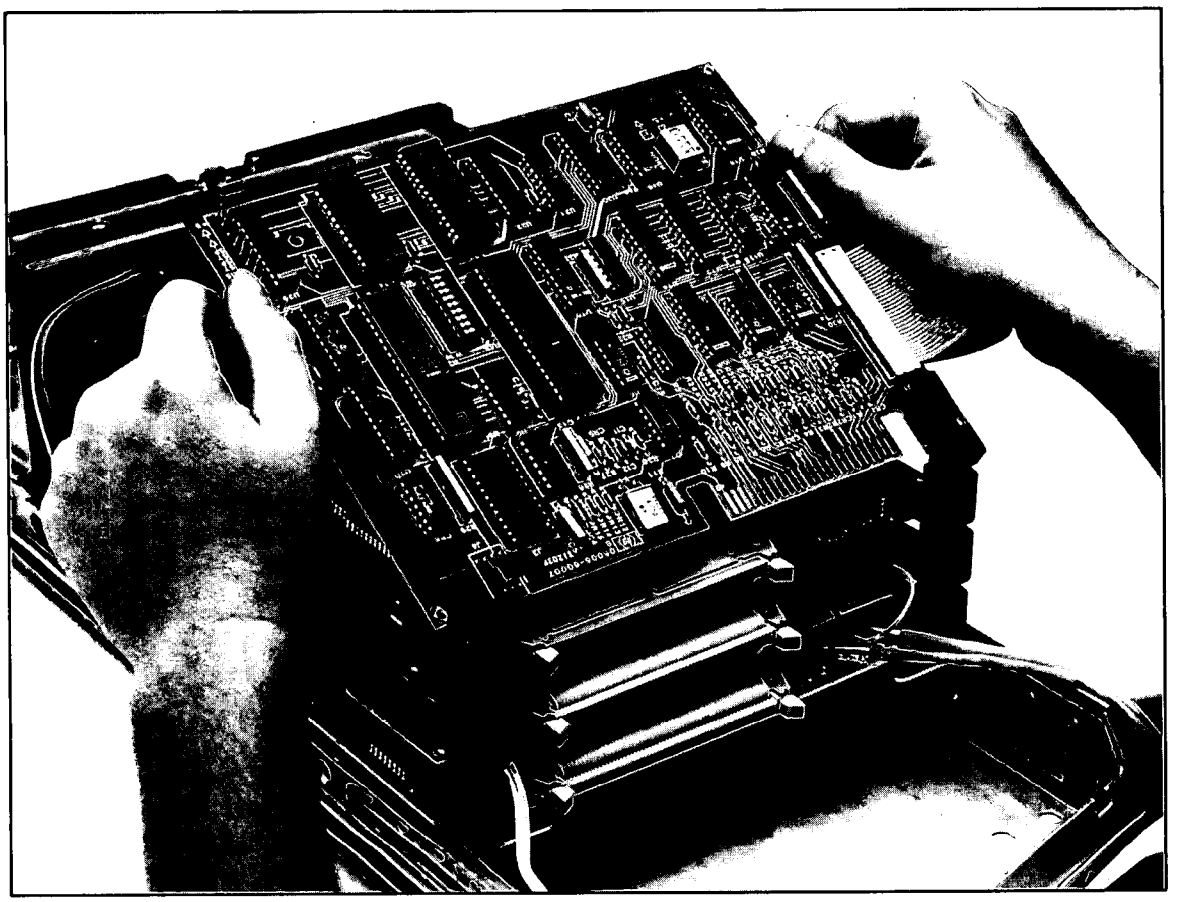


Figure 8-8. Removing A8 HP-IB Assembly

8-83. A3 Microprocessor Assembly Removal

8-84. To remove the A3 Microprocessor Assembly, first remove the A8 HP-IB assembly as described above, then disconnect the 60-line ribbon cable located near the front of the instrument. To disconnect this cable, push the ears of the connector (located at each end) outwards until the ribbon cable unseats. Remove the cable completely by hand. The A3 assembly may now be removed by raising the board on the hinges slightly, and sliding to the right.

8-85. A2 DVM Assembly Removal

8-86. To remove the A2 DVM Assembly, first remove the 60 line ribbon cable and A3 Microprocessor Assembly, as described above. Disconnect the three jumper wires (black, red and green) from the gold posts on A2. Note that the jumpers are color-coded, and that the colors are annotated on A2 and A1. The A2 DVM assembly may now be removed by raising the board on the hinges slightly, and sliding to the right.

WARNING

THE A2 DVM PRINTED CIRCUIT BOARD IS A HIGH IMPEDANCE PC BOARD. IT IS EXTREMELY SENSITIVE TO CONTAMINATION FROM DIRT AND OILS, APPLIED WHEN HANDLING WITH BARE HANDS. CONTAMINATION CAN CAUSE DRIFT, NONLINEARITY, OR INOPERATION. DO NOT HANDLE THE A2 DVM ASSEMBLY WITH BARE FINGERS, EXCEPT AT THE EDGES.

8-87. INSTRUMENT REASSEMBLY

8-88. Reassembly procedures are essentially the reverse of the disassembly procedures. Note that the screws used in chassis assembly should be treated with a liquid thread locking compound (such as LOCTITE®) before reassembly.

8-89. SIGNAL NAMES

8-90. *Table 8-2* is a list of the signal names used in the 5005B. The list is in alphabetical order, and includes the mnemonic used on the schematic diagram. The source, destination, and a description of the function is provided for each signal.

8-91. Ten of the signal lines generated by the A3 Microprocessor Assembly are multiplexed. That is, 10 of the lines have two mnemonic names assigned. These lines are routed from the A3 Microprocessor Assembly to two separate locations on the A1 Main Assembly schematic. Both destinations are identified with the same connector pin number, and are electrically the same point.

®LOCTITE is a registered trademark of LOCTITE Corporation.

Table 8-2. Signal Names

SIGNAL	FROM	TO	DESCRIPTION
a - g, dp a* - g*, dp*	A3J2(34,33, 17, 13, 14, 32, 18, 6)	A4 via A8	Segment drive lines for A4 Display matrix. "*" indicates buffered by A8 assembly.
A - D	A3J1 (11, $\overline{12}$, $\overline{13}$, 13)	A2J1	Binary switch address data for A2 Analog Crosspoint Switches. Code defines the switch which will be set to the state of SW, on the next STROBE.
A1-A5, A7	A9J1 (4, 3, 2, 1, 24, 23)	A8	HP-IB Address Select code lines. A1-A5 are address select. A7 is TALK ONLY Enable.
ALARM	A8J2(41)	A4	Supplies a 2 kHz square wave to activate the ALARM.
$\overline{\text{ATN}}$	A9J1(13)	A8	Attention. Alerts devices on the bus to accept controller data or commands.
B0 - B3	A2J1 ($\overline{4}$, 1, $\overline{5}$, $\overline{6}$)	A3J1	DVM binary output data. Identifies measurement bit.
CLK ↘ EDGE	A3J2 (26)	A4	Drive line for front panel CLOCK falling edge annunciator LED.
CLK ↗ EDGE	A3J2 (27)	A4	Drive line for front panel CLOCK rising edge annunciator LED.
$\overline{\text{COMBINED}}$ $\overline{\text{START/STOP}}$ --- $\overline{\text{SIGN}}$	A3J1 ($\overline{24}$)	A1J1	Control line for A1 Start/Stop Selector. --- Control line for selection of polarity A1 DACs. Lo = 19, Hi = 21.
$\overline{\text{DAV}}$	A9J1(18)	A8	Data Valid. A LOW indicates that the data on the bus is ready to be latched.
DV SIGN	A2J1 ($\overline{7}$)	A3J1	DVM output data polarity status bit.
DEVICE ENABLE 0-7	A3J2 (6, 3, 2, 30, 4, 22, 8, 1, 7)	A4	Column enable lines for A4 Display matrix.
DA0 --- CLOCK EDGE	A3J1 (25)	A1J1	Input data for A1 DAC Address Decoder. Binary weighted value selects one of four DAC enables. --- Control line for A1 synchronizer logic. State determines which input Clock edge is used.
DA1 --- STOP/QUAL EDGE	A3J1 ($\overline{23}$)	A1J1	Input data for A1 DAC Address Decoder. Binary weighted value selects one of four DAC enables. --- Control line for A1 Edge Selector. State determines which input Stop/Qual edge is used.
DATA (PROBE)	A1J1 ($\overline{28}$)	A3J1	Status line for A1 Voltage Comparators. Used to signal comparator transition during offset calibration.
DATA PROBE LIGHT	A1	A5	Probe light enable. A LOW turns the data probe light "ON".
$\overline{\text{DATA PROBE}}$ $\overline{\text{SWITCH}}$	A5	A8	Signal to HP-IB of switch depress. A LOW indicates the switch is depressed.
DIO1-DIO8	A9J1(5, 6, 7, 8, 9, 10, 11, 12)	A8	HP-IB bidirectional data lines.

Table 8-2. Signal Names (Continued)

SIGNAL	FROM	TO	DESCRIPTION
OVOL	A2J1 ($\overline{1}$)	A3J1	Overvoltage. Active high whenever DVM detects an overvoltage input. Flags microprocessor interrupt RST5.5, which isolates the input from the DVM
$\overline{\text{DSTR}}$	A3J1 (20)	A1J1	Data Strobe. Initiates active low enable to one of four A1 DACs, as defined by address lines DA0, DA1.
D1 - D5	A2J1 ($2, \overline{2}, \overline{9}, \overline{10}, \overline{8}$)	A3J1	DVM binary output data. Represents DVM output digit Data.
END OF MEASURE	A1J1 (30)	A3J1	Status line for A1 Stop Measure flip-flop to the A3 microprocessor.
$\overline{\text{EOI}}$	A9J1(22)	A8	End Or Identify. Indicates the end of a multiple byte sequence.
GATE	A1J1 ($\overline{27}$)	A3J1	Status line from A1 Start Measure flip-flop, through U2B, to the A3 microprocessor.
GATE LIGHT	A3J2 (31)	A4	Level shifted GATE line, used to drive front panel GATE annunciator.
$\overline{\text{IFC}}$	A9J1(15)	A8	Interface Clear. A LOW places interface functions in a known quiescent state.
$\overline{\text{K1}}$	A3J1 ($\overline{14}$)	A2J1	Control line for A2 DVM Ohm Control Relay. Low activates relay.
$\overline{\text{K2}}$	A3J1 ($\overline{15}$)	A2J1	Control line for A2 DVM Data/Cal Relay. Low activates relay.
$\overline{\text{K3}}$	A3J1 ($\overline{29}$)	A1J1	Control line for A1 Pull-to-Voltage Relay. Low activates relay.
$\overline{\text{K4}}$	A3J1 ($\overline{30}$)	A1J1	Control line for A1 Data Switch Relay. Low activates relay.
L1-L7 L1*-L7*	A3J1(27, 26, 12, 11, 31, 29, 28)	A4 via A8	Enable lines for LEDs on the "5005B" portion of the A4 Front Panel assembly. "*" indicates signals buffered by the A8 assembly.
LISTEN	A8J2(41)	A4	Enable line for LISTEN LED on A4 assembly.
LSB COUNT	A1J1 (29)	A3J1	Least significant bit from A1 counter prescaler U20B. Combines with REGISTER DATA to produce 17 bits of measurement data.
M/Z	A2J1 ($\overline{3}$)	A3J1	Status line from A2 DVM to A3 microprocessor. Indicates whether the DVM is in Measurement or auto-Zero mode.
$\overline{\text{NDAC}}$	A9J1(16)	A8	Not Data Accepted. Indicates the condition of acceptance of data by the listening device.
$\overline{\text{NRFD}}$	A9J1(17)	A8	Not Read For Data. When HIGH, the listening device will acept input data.
$\overline{\text{OUTPUT}}$ $\overline{\text{SHIFT ENABLE}}$	A3J1 ($\overline{22}$)	A1J1	Control line to reset A1 Measure flip-flops, and enable the FSR to serially output measurement data.

Table 8-2. Signal Names (Continued)

SIGNAL	FROM	TO	DESCRIPTION
$\overline{\text{POP}}$	A3J1 (23)	A1J1	Power on preset, used to initialize A1 synchronizer and tracker flip-flops.
PROBE SWITCH	A8J2(43)	A4	Enable line for PROBE SWITCH LED on A4 assembly.
REGISTER DATA	A1J1 (28)	A3J1	MSB of FSR counter. Used to output measurement data, serially to the A3 Microprocessor. Sixteen bits are output, one at a time, by DATA STROBE.
$\overline{\text{REN}}$	A9J1(14)	A8	Remote Enable. A LOW places the 5005B in REMOTE, a HIGH restores LOCAL control.
$\overline{\text{RESET}}$		A2J1	Resets divide-by-61 counters. Used only during factory board test.
REMOTE	A8J2(50)	A4	Enable line for REMOTE LED on A4 assembly.
SRQ	A8J2(45)	A4	Enable line for SRQ LED on A4 assembly.
$\overline{\text{SRQ}}$	A8J3(19)	A9	Service Request. A LOW alerts the controller to a need for communication.
$\overline{\text{START MEASURE}}$	A3J1 (24)	A1J1	Control line to reset A1 Start Measure flip-flop.
SYNC	A3J1 (26)	A1J1	Control line for A1 Synchronizer Selector U22B. Used to direct the selection of synchronous or asynchronous inputs to Selectors.
START	A3J1 (3)	A2J1	Control line for A1 microprocessor to A2 DVM. Starts A/D conversion.
STROBE	A3J1 (10)	A2J1	Control line from A1 microprocessor to A2 Analog Crosspoint Switches. High state latches in the switch data and address lines, activating the indicated switch.
SW	A3J1 (12)	A2J1	Control bit from A1 microprocessor to A2 Analog Crosspoint Switches. State defines desired condition of addressed switch.
ST ⨍ EDGE	A3J2 (12)	A4	Drive line for front panel START rising edge annunciator LED.
ST ⨍ EDGE	A3J2 (11)	A4	Drive line for front panel START falling edge annunciator LED.
POLARITY DIFF	A3J1 (27)	A1J1	Control line, used during QUAL S.A. to select either the positive or negative Start edge, as the Stop edge.
TD0			Threshold DAC input data bit.
TD1	A3J1 ($\overline{26}$)	A1J1	Threshold DAC input data bit.
START EDGE	A3J1 ($\overline{25}$)	A1J1	Control line, used to route either postive or negative Start edge.
TD2			Threshold DAC input data bit.
DATA STROBE	A3J1 ($\overline{21}$)	A1J1	Control line to shift measurement data, one bit at a time, from the FSR, out REGISTER DATA.
TD3			Threshold DAC input data bit.

Table 8-2. Signal Names (Continued)

SIGNAL	FROM	TO	DESCRIPTION
SIGNATURE-TI — — — — — — — — — TD4	A3J1 (22)	A1J1	Control line for A1 Data/Clock Selector. High during S.A. and T.I. function modes. — — — — — — — — — — — — — — — — — — Threshold DAC input data bit.
TALK	A8J2(39)	A4	Enable line for TALK LED on A4 assembly.
COUNT — — — — — — — — — TD5	A3J1 ($\overline{20}$)	A1J1	Control line for A1 Data/Clock Selector. Low only during S.A. — — — — — — — — — — — — — — — — — — Threshold DAC input data bit.
FREQ-SIGN — — — — — — — — — TD6	A3J1 (21)	A1J1	Control line for A1 Start/Stop Selector. High during S.A. and frequency function modes. — — — — — — — — — — — — — — — — — — Threshold DAC input data bit.
QUAL ENABLE — — — — — — — — — TD7	A3J1 ($\overline{19}$)	A1J1	Control line for S.A. function mode. High during QUAL S.A., Totalize, and frequency. Low during NORM S.A. — — — — — — — — — — — — — — — — — — Threshold DAC input data bit.
UNSTABLE	A3J2 (28)	A4	Drive line for front panel UNSTABLE annunciator LED.
UNCAL	A3J2 (29)	A4	Drive line for front panel UNCAL annunciator LED.
X1-X4 X1*-X4*	A3J2 (10, 24, 5, 20)	A4 via A8	Row enable lines from A1 Keyboard Encoder to A4 Keyboard matrix. "*" indicates buffered by A8 assembly.
XA1-XA4	A8J1(46, 48, 40, XX)	A4	Row enables from A8 Keyboard Encoder to A4 Keyboard matrix. XA1 is used for LOCAL and ALARM VOL keys. XA2 and XA3 are not externally used. XA4 is tied internally to provide Data Probe Switch encoding.
YA1, YA2, YA4	A8J2(42, 44, XX)	A4	Column enable lines from A8 Keyboard Encoder to A4 Keyboard matrix. YA1 and YA2 are used for LOCAL and ALARM VOL keys. YA4 is internally tied to provide Data Probe Switch encoding.
Y1-Y5 Y1*-Y5*	A3J2 (9, 25, 23, 21, 19)	A4 via A8	Column enable lines from A1 Keyboard Encoder to A4 Keyboard matrix. "*" indicates buffered by A8 assembly.
10 MHZ	A3J1 ($\overline{16}$)	A1J1, A2J1	10 Megahertz reference signal from A3 oscillator. Distributed through instrument, and used to generate 5 MHz X1 and X2 microprocessor clocks.

8-92. 5005B THEORY OF OPERATION

8-93. Introduction

8-94. The following paragraphs provide the theory of operation for the 5005B Signature Multimeter. Included is a general instrument description, block diagram description, and the detailed circuit theory.

8-95. General Instrument Description

8-96. The 5005B Signature Multimeter is a multipurpose instrument featuring Signature Analysis as well as frequency, time interval, totalizing, dc voltage, Δ volts, peak volts, and resistance measurement capability. Refer to the Simplified Block Diagram in *Figure 8-9*.

8-97. A microprocessor monitors and directs the overall instrument operation. The microprocessor accesses the onboard RAM and ROMs through the DATA/ADDRESS and CONTROL buses. Data and control instructions for the rest of the instrument are sent and received through the I/O ports of the RAM and ROM modules.

8-98. The measurement function is selected via the front panel keyboard. Pressing any key generally produces a microprocessor interrupt, which alerts the the microprocessor to check the status of the keyboard. The microprocessor then proceeds to configure the various assemblies for the desired measurement, as per instructions stored in ROM. Completed measurements are routed over the DATA/CONTROL lines to the Display.

8-99. Signals are input to the 5005B through the Data Probe and/or the Timing Pod. The Data Probe is used in all functions except the time interval measurement. The Timing Pod is used for Signature Analysis, totalizing, and time interval measurements.

8-100. The Input Signal Switching circuits route the input signals to the appropriate assemblies. The microprocessor controls the signal switching function. The data is passed over the DATA/CONTROL lines. Data can be stored in the RAM, manipulated by the microprocessor, and routed over the DATA/CONTROL lines for display.

8-101. Analog measurements for the volts and ohmmeter functions are performed by the Digital Voltmeter. Digital measurements, including frequency, time interval, totalizing, peak voltage, and signature analysis are performed by the digital measurement circuits.

8-102. The HP-IB Interface and Microprocessor assemblies provide input control and output data of the operation of the 5005B. Signals from the keyboard to the A3 Microprocessor assembly and signals from the A3 assembly to the A4 Display assembly are routed through the HP-IB assembly to provide this I/O capability. In the REMOTE mode, the HP-IB assembly allows an external controller to execute all but one of the functions available from the keyboard. The function not externally controllable is the ALARM VOL control.

8-103. The Simplified Block Diagram in *Figure 8-9* illustrates the relative division of the functional circuits by actual assembly.

8-104. BLOCK DIAGRAM DESCRIPTION

8-105. The following paragaraphs provide a block level description and refer to the Detailed Block Diagram in *Figure 8-18*.

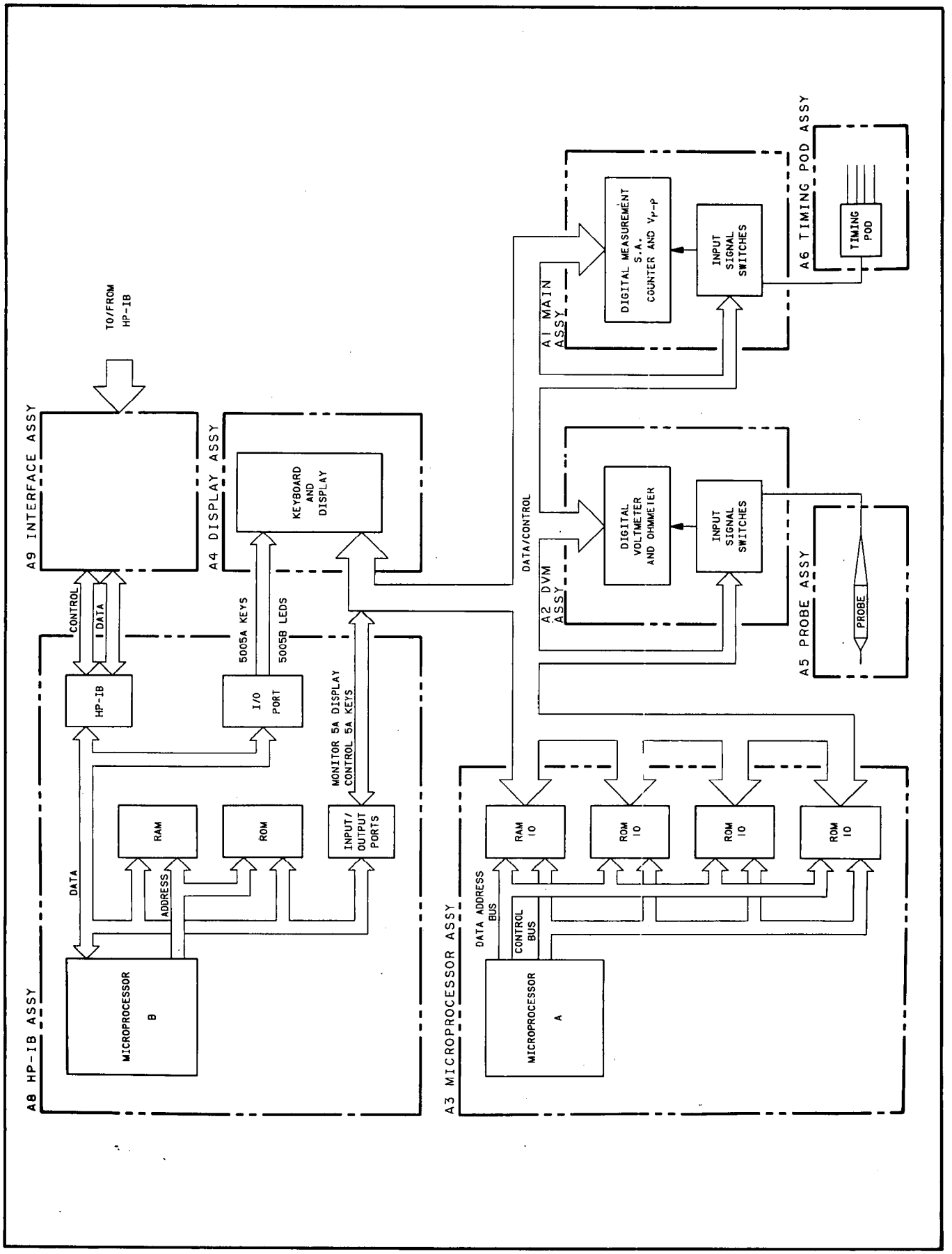


Figure 8-9. 5005B Simplified Block Diagram

8-106. MEASUREMENT TECHNIQUES

8-107. The 5005B makes measurements on both analog and digital signals. During any of the Volts or Ohms function modes, the instrument utilizes analog to digital measurement techniques. During signature analysis, frequency, time interval and totalize function modes, the 5005B operates in a digital mode.

8-108. The Power Supply on the A1 Main Assembly takes the input line voltage and transforms it down to two 20-volt ac sources. These sources are rectified and input to four dc regulator circuits, which provide the ±12.0, +5.0, and -5.2-volt dc supplies used throughout the instrument.

8-109. Depending on the selected function mode, input signals are received through the A5 Data Probe and/or the A6 Timing Pod assemblies. The Data Probe and Timing Pod input assemblies attenuate the input signals by a factor of 10 via passive divider networks. Signals from the Timing Pod are fed directly to the Input Voltage comparators on the A1 Main assembly. Signals from the Data Probe are routed through the Data Switch relay to the Input Voltage comparators. The reference threshold voltages for the high-speed voltage comparators are generated by four Trigger Threshold DACs (Digital-to-Analog Converters). The DACs transform digital threshold information which is determined by the front panel control settings and stored in RAM (ROM for default values), into the analog reference threshold voltages. The value of the threshold voltage determines the logic family and trigger levels of the signals at the inputs.

8-110. The outputs of the respective voltage comparators are level-shifted via ECL-to-TTL translators and routed through Synchronizing and Edge-Select circuits. The Edge-Select circuits, directed by the front panel data, determine which transitions of the Data Probe, START, STOP, and CLOCK signals are used for measurement timing, and also determine the polarity level of the QUAL input signal. The output of the Data Probe comparator also drives the Data Probe light driver, which detects either logic high, logic low, three-state, or active data states of the probe. These conditions are displayed either by lighting, extinguishing, dimly lighting, or flashing the Logic State Indicator lamp within the Data Probe tip.

8-111. After edge-selection, the signals are routed through the Data and Clock Selector Logic circuits to the Feedback Shift Register/Counter (FSR) circuits. The microprocessor, responding to front panel data, directs the Selector logic to route specific signals to the circuits required to perform the desired measurement. The configuration of the Selector logic, along with the operating mode of the FSR, determines the measurement function. The microprocessor controls the Selector logic and configures the FSR. The FSR can be configured as a shift-register or a standard accumulating counter, depending on the measurement. The possible configurations and operating modes of the FSR are as follows:

a. During both Signature Analysis modes (NORM and QUAL), the FSR is configured as a shift-register with feedback. This configuration, referred to as a pseudo-random-bit-sequencer counter (PRBS), allows the FSR to perform the S. A. measurement algorithm.

b. After all measurements, the FSR is automatically reconfigured as a serial shift-register, which is used by the microprocessor to read out accumulated or residue measurement data. The data is serially output to the microprocessor system, where it is processed, formatted, and routed to the Display Decoder Driver. The Display Decoder Driver receives, decodes, and then displays the result.

c. During frequency and time interval measurements, the FSR is configured as an accumulating counter. For frequency measurements, the Selector Logic routes the Data Probe input into the counters, and gates the data in for the 5005B's preset one second gate period. For time interval measurements, the internal 10 MHz clock (produced by the 10 MHz Clock Generator on A3) is routed into the counters, and is accumulated for the duration between the Start and Stop inputs on the Timing Pod.

8-112. For analog inputs during voltage measurements, dc voltage applied to the A5 Data Probe is routed through input relays on A1, through the DVM relays on A2, and on to the attenuator, which if necessary, can divide the voltage by a factor of 10 or 100. After attenuation, the voltage is routed to the analog section of the Analog-to-Digital Converter where it is converted to digital data, using the sucessive approximation method. The Digital section then generates the appropriate Digit, Sign, and 4-bit BCD code information which is sent, via the I/O, to the microprocessor. The microprocessor decodes, processes, and sends the information to the Display Decoder Driver circuits, which in turn route it to the A4 Display Assembly where the data is displayed.

8-113. The Analog Crosspoint switches on A2 form a 4 × 4 switch matrix, which is used to route analog calibration voltages, and activate the appropriate attenuation circuit. The microprocessor determines the selections and controls the switch.

8-114. Resistance measurements are performed by comparing the voltage across a known calibration resistor with the voltage across the unknown resistance (between the Data Probe tip and ground). The known calibration resistor (Reference Resistance) is located within the Data Probe. The 2.0 Volt Reference Generator on A2 is used with the Reference Resistance to generate the reference voltage. The DVM measures the voltage, and the unknown resistance is computed by the microprocessor. Overvoltage protection is provided, via relays, in case the Data Probe is mistakenly placed across a voltage source while in a resistance function. When OVOL (from the A2 Overvoltage Detector) goes HIGH, Reset 5.5 on the Microprocessor is pulled HIGH, which causes the A2 K1 and K2 relays to be activated, isolating the Data Probe and DVM from the source.

8-115. FUNCTION MODE DESCRIPTIONS

8-116. The microprocessor responds to Keyboard interrupts by reviewing the status of all front panel keys. The microprocessor directs the Keyboard Encoder circuits on A3 to scan the keyboard matrix on A4, and stores the results in RAM. This allows the microprocessor, by using the Selector Logic, Relays, and Analog Crosspoint Switches, to configure the instrument circuitry for any selected function mode and parameters. The following paragraphs describe the basic measurement configuration for each of the major function modes, and refer to the Detailed Block Diagram in *Figure 8-18.*

8-117. In general, pressing any front panel key will cause a microprocessor interrupt condition to occur. The microprocessor will respond by identifying the activated key and configuring the instrument accordingly. The categories of possible key selections during most function modes are as follows:

- Mode change
- Edge or Level Select change
- Logic Family and/or Threshold Adjustment change

a. A Mode change occurs when the user presses a FUNCTION key other than the current operating mode. The microprocessor automatically senses the key selection and reconfigures the instrument to the selected mode.

b. An Edge Select change or Level Select change occurs when one of the front panel POLARITY keys is pressed. This causes the microprocessor to reprogram the Edge Select and Level Select circuitry on the A1 Main Assembly to respond only to the set conditions. Note that only the edges or levels used in the currently active function mode (as indicated by lighted front panel LEDs) are affected.

c. Threshold reading request or level change occurs when one of the currently active THRESHOLD keys are depressed. Note that only the thresholds currently being used have their LED indicators lighted. When a threshold reading request is activated (by a keypress within the THRESHOLD section) the microprocessor recalls the currently active

threshold setting and displays it on the front panel, with the appropriate H (for HIGH logic state) or L (for LOW logic state) designations. The operator can change the active threshold level by changing logic families or by pressing the slew keys (with arrows) when the thresholds are being displayed. Internally, the microprocessor interprets the keypresses and programs the DACs on the A1 Mainboard to the new active levels.

An intermediate or "null" logic level, used during Signature Analysis by the Data Probe, is produced by the Pull-to-Voltage Generator. The active logic levels selected for the Data Probe by the Trigger Threshold DACs drive the analog divider circuits within the Pull-to-Voltage Generator. The output is a buffered level at the midpoint (or logic null) between the HIGH and LOW logic levels.

8-118. Signature Analysis Mode

8-119. Two modes of Signature Analysis operation are provided: NORM and QUAL. In the NORM mode of operation, the START signal comes from the START/ST/SP input and the STOP signal comes from the STOP/QUAL input of the 5005B Timing Pod. In the QUAL mode, both the START and STOP signals come from the START/ST/SP input and the QUAL signal comes from the STOP/QUAL input of the Timing Pod. This allows the framing of data within an operator specified Signature window.

8-120. SIGNATURE ANALYSIS/NORM MODE. During the NORM Signature Analysis mode, the input relays are programmed to route data from the Data Probe, and timing signals from the Timing Pod, to the Data and Clock Selector logic. The timing signals pass through Synchronizing and Edge Select circuits to the Data and Clock Selector circuits. After conditioning by these circuits, the data is routed to the Feedback Shift Register where the Signature Analysis algorithm is performed. This data is read at the end of the measurement by the microprocessor through a serial data link from the A1 Main Assembly.

8-121. SIGNATURE ANALYSIS/QUAL MODE. The operation of the QUAL Signature Analysis mode is similar to the NORM mode, except that the START and STOP inputs are input on one line, and the measurement is "windowed" (gated) by the status of the QUAL input. The data is still input through the A5 Data Probe, and the algorithm performed by the Feedback Shift Register remains the same.

8-122. kHz Mode

8-123. In the kHz Mode, the edge-select and threshold-select routines are performed as previously described for the desired levels. The Data Probe is the only active input in this mode. The microprocessor programs the input relays to route data to the Feedback Shift Register which is reconfigured by the microprocessor to be a totalizing counter. The microprocessor counts the number of overflows that occur, and the residue in the counter at the end of the measurement. It computes the total number of events during the fixed one second gate and displays this number as the frequency of the input. The gate light is flashed at a 1 Hz rate to indicate this gating function.

8-124. TOTLZ Mode

8-125. The TOTLZ Mode is similar to the kHz mode except the START and STOP inputs on the Timing Pod are used to select the gate time instead of utilizing the fixed 1 second gate. The counter's contents are read at the end of the measurement, and the number contained is formatted and displayed.

8-126. ms Mode

8-127. The ms (Time Interval) mode uses the START and STOP signals from the Timing Pod to gate the 10 MHz time base into the counter section. The time base pulses are totalized for a duration determined by the Start and Stop pulses. The microprocessor is interrupted when an overflow occurs. The total number of overflows that occur between the Start and Stop pulses are accumulated in one of the microprocessor's internal registers. The residual time base pulses are contained in the Feedback Shift Register. This number is read at the end of the measurement by the microprocessor and a time interval is computed and displayed.

8-128. DCV Mode

8-129. In the DCV (DC volts) mode, the microprocessor configures the A1 input relays so the voltage at the Data Probe tip appears at the Data/Cal Relay of the A2 DVM assembly. The Data/Cal relay routes the signal past two switchable attenuators to the A/D Converter within the DVM. The attenuators are controlled by the Analog Crosspoint Switch under the direction of the microprocessor. The signal is either attenuated by X10 or X100. The selected attenuation factor is determined by the autoranging algorithm, stored in ROM. The Analog Section of the A/D Converter, in conjunction with the Digital Section, computes the voltage of the input. The DVM uses the precision 10.00 volt reference for an input for the measurement and the 10 MHz timebase signal (divided by 61) for timing purposes. At the end of the measurement the computed voltage is acquired by the microprocessor which formats and displays the results of the measurement.

8-130. The incoming signal is checked by the Overvoltage Detector for excessive voltage. If the voltage extremes at the Overvoltage Detector circuit are more positive than +2.95 volts or more negative than +0.9 volts respectively, the microprocessor is flagged. The microprocessor immediately responds by isolating the probe from the 5005B, via a relay. The Overvoltage mnemonic (OL/OLOL) is displayed, while the instrument waits a fixed time interval before attempting the measurement again.

8-131. ΔV Mode

8-132. The Delta Volts Mode is similar to the DCV mode, except that the microprocessor accepts the first voltage measurement (performed when the ΔV key is pressed) as the reference. This voltage value is stored, then subtracted from the result of each successive measurement. The difference value is then displayed.

8-133. KΩ Mode

8-134. The K Ohms mode utilizes the voltmeter to produce a resistance measurement. The Precision 10.00 volt source is divided to obtain a Precision 2.00 volt source. The 2.00 volt source drives a 20 K ohm resistor placed in series with the unknown resistance to ground. This is achieved via the Data Probe with the programmed relays. The DVM circuits compute the voltage at the node between the 20 K ohm resistor and the unknown. The microprocessor acquires the voltage and proportionally computes the unknown resistance.

8-135. V_P+ and V_P- Mode

8-136. For the V_P+ and V_P- modes, the input signal is routed via the input relays to the Input Voltage Comparators. The Trigger Threshold DACs are programmed by the microprocessor to find the peaks of the incoming signal. This is achieved with a successive approximation method of outputting incremental voltages by the DACs until the comparators change state or trigger. This trigger point is displayed by the microprocessor. Note that the microprocessor knows the trigger point because it keeps a record of the programmed DAC voltage.

8-137. DETAILED CIRCUIT THEORY

8-138. The following paragraphs provide the detailed circuit theory for each assembly within the 5005B. The theories are presented in numeric order, by assembly number, and reference the individual assembly schematic diagrams in *Figures 8-19* through *8-24*.

8-139. A1 MAIN ASSEMBLY

8-140. The A1 Main Assembly contains the Power Supply, Input Circuitry, Trigger Threshold DACs, Edge-Select and Synchronization circuits, Data and Clock Selector Logic, and the Feedback Shift Register.

8-141. Power Supply

8-142. The 5005B power supply provides six dc voltages: an unregulated + and -20 volts as regulated +5, -5.2, +12, and -12 volts. Power transformer T1 converts the line voltage input from the A7 Line Module into two 14V ac secondary voltages. Each secondary is rectified with a full-wave bridge network, CR5 and CR6, providing an unregulated -20V dc and +20V dc, respectively. The unregulated +20 volt line feeds +12 volt regulator VR3, and the +5 volt regulator circuitry U25, Q2, and CR8. VR3 is a simple three terminal regulator. U25 and its support circuitry form a switching type regulator for the +5 volt power.

8-143. U25 monitors the +5 volt output, through the R62/R64 resistive divider, at pin 16. The dc level at pin 16, typically +4.9 volts, controls the variable duty cycle of the ~25 KHz pulse train output at U25, pins 8 and 11. The pulse train drives the base of switching transistor Q2, through R57. The duty cycle of the pulse train determines the amount of time Q2 is switched on and off, thereby regulating the amount of current supplied by the +5 volt supply. Should the supply be loaded down, the dc level at U25 pin 16 would drop, causing the duty cycle at pins 8 and 11 to change, remaining low for a longer percentage of time. Q2 would be switched on proportionally longer, supplying the additional current to the load. When the load is removed, the regulator returns to its quiescent operating condition. Diode CR8 is an over voltage protection diode limiting the output to six volts. Resistor R52 is used to eliminate start-up problems associated with pin 1 falling below ground. On start-up, R52 keeps pin 1 and 15 of U25 (TL494) above ground. Inductor L2 is the primary energy storage device and diode CR7 provides a current path when Q2 is shut-off. The unregulated -20 volts feeds the three terminal -12 volt regulator VR1, which in turn feeds the -5.2 volt regulator VR2.

8-144. Input Circuitry

8-145. The A1 Main Assembly receives the four main input signals, DATA, START/ST/SP, STOP/QUAL, and CLOCK, from the A5 Data Probe and A6 Timing Pod. The three signals from the Timing Pod, START/ST/SP, STOP/QUAL, and CLOCK, are directly fed to the positive inputs of Input Voltage Comparators U6C, U6D, and U6E, respectively. The Data Probe signal is routed through the Data Switch Relay K2, to the positive inputs of U6A and U6B. The alternate output of the dual N.O./N.C. relay routes the Data Probe signal to the A2 DVM Assembly during volt and ohmmeter functions. The Pull-to-Voltage Relay, K1, is used to route reference voltage to the 20K ohm reference resistor within the A5 Data Probe during the ohmmeter function. The input relays are controlled via the microprocessor by control lines $\overline{K3}$ and $\overline{K4}$.

8-146. Variable capacitors C7 through C10, along with their resistive networks, provide adjustable input compensation for the four input signals. These circuits allow the input response to be tuned for minimum overshoot and undershoot. The negative (or reference) inputs for the Input Voltage Comparators come from the Trigger Thresholds DACs, described in following paragraphs. The outputs of the Input Voltage Comparators are routed through ECL/TTL logic translators U11 and U12, to their individual Edge-Select, U17A-D, and Synchronizer, U18 and

U21, circuits. The signals are then input to the Selector Logic, which configures the signals for the desired measurement. The Selector Logic includes the DATA and CLOCK Selector, U3, and the START/STOP Selector, U16.

8-147. Trigger Threshold DACs

8-148. The four Trigger Threshold DACs, U1, U4, U7, and U13, transform digital information from the microprocessor into analog voltage, used by the input circuits to set the individual logic thresholds. The DAC inputs are connected in parallel. Eight bits of digital information are placed on lines TD0-TD7 by the microprocessor. Control lines DA0 and DA1 set up DAC Address Decoder U2 (a one-of-four decoder) whose outputs drive the latch enables (pin 10) of each DAC. When the data strobe line $\overline{\text{DSTR}}$ goes low, the DAC threshold data is latched into the desired DAC. Each DAC has dual-polarity current outputs, which drive Op-amps, U14A through D, configured as current-to-voltage translators. The outputs of the Op-amps are routed through resistor voltage-dividers and filters, to the negative (or reference) inputs of the five high-speed Input Voltage Comparators, U6A-E. The circuit configuration allows for a single separate programmed threshold level for the Clock, via U13; the Start and Stop inputs, via U7, and two threshold levels (logic high and logic low) for the Data Probe input, via U1 and U4.

8-149. During DVM modes, the Data Switch Relay, K2, is activated, routing the dc voltage level to the A2 DVM assembly through A1W2. The positive inputs to the Input Voltage Comparators are effectively pulled to ground through 10 KΩ resistors. The microprocessor, between voltage measurements, manipulates the DAC input data lines, performing a successive approximation routine, looking for the change of state level. Since the positive inputs are tied to ground, the voltage at which the comparators switch represents zero offset (the threshold level error due to leakage through the 10 KΩ resistors). The change of state from each comparator is routed through the ECL/TTL translators, U11 and U12, through threshold synchronizer U18 and Edge Selector U17C, to the Main Data Path. The DATA (PROBE) signal taps off Main Data Path, and is output on J1 pin $\overline{28}$ to the A3 Assembly, where it signals the microprocessor that the zero offset has been found. The offset values, determined for each comparator, are stored on the A3 Microprocessor Assembly, and recalled and inserted as correction factors during the generation of input threshold levels.

8-150. Feedback Shift Register and Control Logic

8-151. The Feedback Shift Register (FSR) is comprised of four synchronous binary counters, U8, U9, U15 and U19, basically configured as a shift register (i.e., A output to B input). Exclusive OR/NOR gates, U5C and D, allow feedback of selected bits from each stage of the FSR to the inputs of the first two counters, U8 (pin 3) and U9 (pin 3), forming a pseudo-random-bit-sequencer counter. During standard count modes, the FSR is set up as a divide-by-two (to the 16th) counter. F/F U20B acts as a divide-by-two prescaler to the FSR, producing a divide-by-two (to the 17th) counter, whose least significant bit is output by U20B (pin 9).

8-152. The FSR is used to accumulate and modify data in digital measurement modes. The actual operation of the FSR varies slightly, dependent upon the selected function mode. The following paragraphs describe the useage of the FSR during the three primary measurement configurations: Signature Analysis, Frequency and Time, and Data Read functions.

8-153. Signature Analysis Function

8-154. Three timing signals are required to make Signature Analysis (SA) measurements on data streams through the Data Probe: Clock, Start, and Stop.

8-155. The Clock signal, input through the Timing Pod, enters the A1 Main Assembly through R2 to the positive input of Voltage Comparator U6E (pin 19). The negative input (pin 14) of U6E is the threshold reference input. This threshold reference voltage is provided by the Clock DAC U13, under control of the microprocessor, and represents the front panel threshold level selection. The detected clock, from U6 (pin 17), goes to the inverting input of the ECL/TTL translator U11B. The level-shifted clock signal then goes to the clock Edge-Selector U17D (pin 12). U17D is an exclusive-OR, which passes either a normal or inverted version of the input signal, determined by the CLOCK EDGE signal on U17 (pin 25). When the CLOCK EDGE line is HIGH, U17D acts as an inverter. When it is LOW, the clock signal is passed unchanged. The output of the Edge-Selector U17D (pin 11) is routed to the Clock Selector, U3 (pin 11). The Clock Selector is controlled by the microprocessor through control lines COUNT and SIGNATURE-TI. When COUNT is LOW and SIGNATURE-TI is HIGH (binary 01), U3's number "one" input lines (pins 5 and 11) are selected. The Clock Selector, U3, output (pin 9) drives the clock inputs (pins 2) of the FSR counters U8, U9, U15, and U19.

8-156. Start and Stop signals are required to define the measurement window. In the NORM Signature Analysis mode, the Start signal is input through the A6 Timing Pod to the Voltage Comparator U6C (pin 5). The Voltage Comparator output (pin 10) goes through ECL/TTL translator U11C, to Edge-Selector U17B, which either inverts the signal or passes it directly, depending on the level of START EDGE, at U17B (pin 5). When START EDGE is HIGH, U17B acts as an inverter. When START EDGE is LOW, the signal is passed unchanged. After edge-selection, the signal is inverted by U5B, and input to the Start/Stop Synchronizer U21A. The true and complemented signals at pins 6 and 7 of U5B are utilized as asynchronous start and stop signals during T.I. and Totalize functions. The true and complemented signals at pins 5 and 6 of U21A are synchronous to the Main Clock and are utilized during Frequency, Period, and NORM Signature Analysis modes. The four Start/Stop signals are input to the Start/Stop Selector U16 (pins 12, 13, 14, 15). The output of the Start/Stop Selector, U16, clocks control flip-flops U10A, U10B, and U20A. U10B output (pin 9) goes HIGH, which removes the Reset condition from all four FSR counters (U8, U9, U15, and U19), which enables them to start the measurement. The complemented output of U10B (pin 8) is inverted through U2B, and output as GATE on J1 pin $\overline{27}$. This signal is routed through the A3 assembly to the A5 Display, where it drives the front panel Gate LED.

8-157. The Stop signal is input through the A6 Timing Pod to the Input Voltage Compararator U6D (pin 8). The Voltage Comparator output (pin 11) goes through ECL/TTL translator U11D to the Edge-Selector U17A. The STOP/QUAL EDGE line determines whether the Stop signal is inverted or passed unchanged. After edge-selection, the signal is routed to the Start/Stop Selector, U16 (pins 3,4), and to exclusive-OR/NOR U5A. Pin 1 of U5 is tied to ground, so the Stop signal is passed unchanged to the data input of the Start/Stop Synchronizer, U21B (pin 12). U21 synchronizes the Stop signal to the Clock. The synchronized Stop signal passes from U21B (pin 9) to the Start/Stop Selector U16 (pins 1,2). The selected Stop output from U16 clocks control flip-flops U10A,B and U20A, sending U10A (pin 5) HIGH, which produces END OF MEASURE (J1 pin 30). This flags the microprocessor, signaling the measurement is complete. When U10 pin 5 goes HIGH, pin 6 goes LOW, which disables the FSR counters (U8, U9, U15, and U19) through OR gate U26D.

8-158. In the QUAL mode, the Stop signal is input through the A6 Timing Pod, on the same line as Start (START/ST/SP). Both the Start and Stop signals are processed through the same input circuits up to the Start/Stop Synchronizer. U21A becomes the synchronizer for both the Start and Stop signals. The outputs from U21A (pins 5 and 6) are the true and complemented Start signals. These signals are input to the Start/Stop Selector on pins 12 and 13. The control line POLARITY DIFF works in conjunction with START EDGE to select either the positive or negative Start Edge as the desired Stop Edge during QUAL SA. POLARITY DIFF comes in through U26C, to pin 11 of the Start/Stop Selector U16. Pin 11 is the LSB of the binary select lines, determining whether an odd or even input is selected, whether pin 13, the true Start Edge, or pin 12, the complemented Start

Edge, is selected. $\overline{\text{COMBINED START/STOP}}$ goes LOW, enabling U26B, which allows selection of the four higher order inputs (4 through 7) by the Start/Stop Selector.

8-159. The QUAL input comes in through U6D and U11D, to Edge-Selector U17A. The output at pin 6 goes through Exclusive OR/NOR U5A, and passes unchanged to the data input of the Start/Stop Synchronizer U21B. QUAL ENABLE goes HIGH in the QUAL mode, enabling gate U26A to pass the QUAL signal through as enable (LOW) or disable (HIGH) for the FSR counters.

8-160. Frequency and Time Interval Functions

8-161. The Frequency, Time Interval, and Totalize functions are similar, in that the FSR is configured as an accumulating counter, counting asynchronous events input through the A5 Data Probe. The differences are in the methods of gating the FSR. For Frequency, the FSR is gated through timer circuitry on the A3 Assembly, which generates one second gate periods between readouts. The Time Interval and Totalize modes use external Start and Stop signals, through the A6 Timing Pod, to window the measurement.

8-162. During a frequency measurement, the signal is input through the A5 Data Probe, through the Data Switch Relay K2, to the Input Voltage Comparators. Two voltage comparators, U6A and U6B, are required for the Data Probe input signal. This allows DAC threshold control over both the HIGH and LOW logic level for all logic families. The outputs of U6A and U6B represent the duty cycles of the active LOW and HIGH trigger thresholds. These outputs are level-shifted through ECL/TTL translator U12B and U12C, and input to the "J" and "K" inputs of the Probe Synchronizer U18A and U18B. The output of U6A is also routed through ECL/TTL translator U11A, whose output helps drive the Data Probe Light Driver U24. U18 is not used for synchronization in this mode, but rather configured as an RS F/F, setting and resetting on the edges of the HIGH and (inverted) LOW data probe signals, through U22A. U22A is a 2-to-1 data selector, controlled by the SYNC line from the microprocessor, used to determine the Set and Reset for U18A and U18B. U18B is not used in the frequency mode.

8-163. The resulting output from U18A (pin 5) is a waveform representing the duty cycle of the active triggering period. The output from pin 6 is the true facsimile of the input signal. This output is routed directly to pin 4 of the Data Selector U3. The Data Selector directs input "1" during S.A., input "2" during Frequency, and input "3" during T.I. The selected output is routed through U5C, as input to the Feedback Shift Register.

8-164. During a Time Interval measurement, the Start and Stop signals enter the Timing Pod, and are processed just as the NORM S.A. measurement mode. These signals define the measurement counting window. Microprocessor control lines SIGNATURE-TI and COUNT will be HIGH, causing Data Selector U3 to route the internal 10 MHz Oscillator signal to the FSR counters. The FSR, configured as a counter, will accumulate 10 MHz clock pulses for the duration set by Start and Stop. After the Stop is received, END OF MEASURE is generated, signaling the microprocessor to perform a Data Read on the counters.

8-165. Data Read Function

8-166. After any measurement, 16 bits of data are serially read out of the FSR on U19 (pin 11), and output as REGISTER DATA on J1(28), into the microprocessor system at A3U4 (pin 34). When in count modes, the seventeenth bit is developed by flip-flop U20B and output as LSB COUNT on J1(29).

8-167. Coincident with the Stop signal is the END OF MEASURE signal from U10A (pin 5). A high on this flag signals the microprocessor that the measurement is complete. The microprocessor sends QUAL ENABLE LOW, forcing U26A HIGH and U26D LOW, enabling the shift mode on FSR counters U8, U9, U15 and U19. The microprocessor reads the LSB COUNT line, from U20B (pin 9),

and $\overline{\text{OUTPUT SHIFT ENABLE}}$ goes LOW, which resets U10A, clearing END OF MEASURE (pin 5). DATA STROBE, from the microprocessor, is then routed by Clock Selector U3, to clock the data out of U8, U9, U15, and U19 through U19 (pin 11). Each DATA STROBE pulse moves one bit out of the FSR.

8-168. During count modes, the FSR is configured as a divide-by-two (to the sixteenth), with an additional bit of resolution (divide-by-two to the seventeenth) provided through divide-by-two prescaler U20B. Normal inputs can overflow the counting ability of this configuration. The microprocessor provides an interrupt every 250 microseconds. During that interrupt, the REGISTER DATA bit (MSD) is examined. Whenever a transition is detected, indicating the counter is full, the microprocessor assumes an overflow has occurred, and stores the overload bit within an internal register. The count in the counter rolls over to all zeros with the next clock. At the end of the measurement, the number of overflows is combined with the residue count in the FSR to calculate the total number of events.

8-169. The GATE output (pin $\overline{27}$) basically monitors the Measure Flip-Flop U10B when a measurement is in progress, and determines when the FSR is accepting data. The GATE signal is routed through A3, to the A4 Display Assembly, where it drives the Gate Light LED.

8-170. A2 DVM ASSEMBLY

8-171. The A2 DVM Assembly contains the circuitry necessary for the voltage and resistance measurement functions of the 5005B. The A2 DVM Assembly contains the input DVM relays, Attenuators, Clock Divider, A/D Converter, Analog Crosspoint Switch, and various protection and voltage reference circuits.

8-172. A/D Converter

8-173. The basic function of a voltmeter is to convert an analog input voltage level to digital data, which can then be processed and displayed by the microprocessor system. This function is performed by two LSI chips, U4 and U7, which form a 4 1/2 digit A/D Converter. U4 is the Analog Section and U7 is the Digital Section.

8-174. The A/D Converter desired measurement input voltage range is from -2.5 to +2.5 volts, at its input U4 (pin 15). Two attenuators allow the input voltage to be scaled by a factor of 10 or 100. This configuration allows three ranges of input voltage; ± 2.5 volts, ± 25 volts, and ± 250 volts, depending on which, if any, attenuators are active. At no time does the actual voltage to the A/D Converter circuits exceed ±5.0 volts, due to the voltage clamps internal to U10.

8-175. During a voltmeter function, one of the attenuators is always on, selecting either the ±25 volt (X10) or ±250 volt (X100) range. The 2.5 volt range (no attenuation) is only used during the ohmmeter function. If the DVM's first measurement is greater than ±2.5 volts, the microprocessor will direct the Analog Crosspoint Switch to turn off the X10 attenuator and turn on the X100 attenator. This autoranges the voltmeter from the ±25 volt range to the ±250 volt range.

8-176. The attenuated input voltage appears at U4 (pin 15) via buffer amp U10. The +8 volt reference at U4 (pin 10) REF IN, is formed by the resistive voltage divider of R9, R10, and R8. The buffered REF OUT, U4 (pin 8), goes through R17 to the integrator input at U4 (pin 9).

8-177. The digital section of the A/D Converter is U7. With its input from U4, the data output of U7 is on four BCD lines, digit available on five lines, and Sign information. The BCD outputs are at U7 pins 9, 10, 11, and 12 with the LSB (B0) at pin 9. The Digit Available, D1 through D5, are output at pins 2, 1, 18, 17, and 16, respectively. The Sign output is at pin 13 and when HIGH, indicates a positive voltage reading. The Start input to U7 is at pin 7 and comes from the microprocessor. The final input to U7 is the clock. The clock is approximately 164 kHz, generated by U8 and U9. U8 and

U9 are connected to form a divide-by-61 circuit. The input to this circuit is pin 2, the internal 10 MHz clock. The 164 kHz output is U9 (pin 13) which goes through level shifter Q6 to the "fOSC" input of U7 (pin 8).

8-178. Voltmeter Function

8-179. During the Voltmeter function, input dc voltage enters through the A5 Data Probe tip, and is routed to the A2 DVM assembly by the Data Switch Relay on A1. The voltage enters A2 at J2, transfers through the DVM DATA/CAL Relay K2, through series resistor R5, through buffer amplifier U10, to the V_{IN} input of U4 (pin 15). The input of U10 clamps the input line to ±5 volts to prevent a dc level greater than 5 volts from reaching the input of U4. The FET circuits Q4/R6 and Q3/R7 form the X10 and X100 Attenuators. *Table 8-3* shows the Attenuator control for each of the three ranges. The attenuators are activated via the Analog Crosspoint Switch, which decodes binary information from the microprocessor system, directing either +10.00 volts or GND to the gate of the desired FET. Switching GND to a FET will turn it ON (saturation), switching +10.00 volts will turn it OFF.

Table 8-3. DVM Range Setting

INPUT VOLTAGE RANGE	ATTENUATOR	Q4	Q3	U2 SWITCH ACTIVATED	
2.5000V (OHMS Mode)	(X1)	OFF	OFF	S1	S2
25.000V	X10	ON	OFF	S13	S2
250.00V	X100	OFF	ON	S1	S14

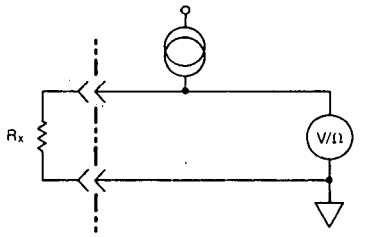
8-180. In the 25 volt range, Q4 is turned ON placing R6 in the circuit. The combination of A5R1 (89.6K), A2R5 (10M), and R6 (1.1M) forms a 10:1 voltage divider which attenuates the input by 10. In the 250 volt range, Q4 is turned OFF and Q3 is turned ON, placing R7 in the circuit. The combination of A5R1 (89.6K), R5 (10M), and R7 (100K) form a 100:1 voltage divider which attenuates the input by 100. In the 2.5 volt range, both attenuator FETs are turned OFF.

8-181. Analog Crosspoint Switch

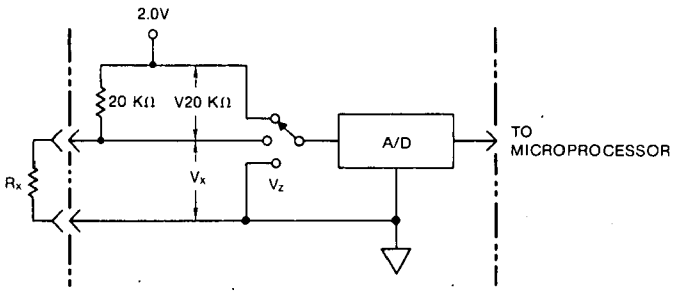
8-182. The enabling of attenuators Q3 and Q4 and the switching of calibrate voltages is performed by U2, which is a 4 × 4 Analog Crosspoint Switch. The microprocessor controls U2, through level shifter U5, by: setting the switch address on lines A, B, C, and D (U2 pins 6, 5, 3, and 4), setting the desired switch status on SW, U2 pin 2 (1 for ON or 0 for OFF), and strobing this data through SW, pin 7. For example, when the voltage range is switched to the 25.00 V range, Q4 is turned on, causing the input voltage to be divided by 10. The microprocessor then addresses U2 (switch 13) by placing 1101 on pins 4, 3, 5, and 6 respectively. Next, the microprocessor sends a clock to the SW input U2 pin 7. This causes switch 13 to close, allowing GND to be applied to the gate of Q4 which turns ON, placing R6 (1.1M) into the circuit which causes the input voltage to be divided by 10.

8-183. Ohmmeter Function

8-184. In most ohmmeters, a constant-current source is output to the unknown resistor (Rx) and the voltage developed across Rx is then measured and displayed in ohms, as illustrated in the diagram below.



8-185. The disadvantages of this method are: (1) The current source must be precision and (2) there is limited range. The 5005B uses an alternate method which overcomes these disadvantages. The diagram below is the simplified circuit used by the 5005B.



8-186. The 5005B uses a 2.0V source and a resistor of known value. When measuring ohms, the voltage across the known 20.00K resistor is measured and the value is stored. Then, the voltage across the unknown resistor, Rx, is measured and stored. The microprocessor then determines the ratio of the two voltages and computes and displays the resistance value using the following formula:

$$Rx = \left(\frac{Vx - Vz}{2.0V - Vx} \right) 20K \text{ ohms}$$

Where: Rx = Unknown Resistance
Vx = Voltage measured across Rx
Vz = Zero voltage (Ground)
2.0V = 2.0V reference

8-187. The circuits involved include U3, K1, and K2 on the DVM Assembly and R2 on the Data Probe. U3 acts as a buffer for the 2.0V source. The output of U3 (pin 6) goes through Ohm Control Relay K1 to Rx via the 20.00K resistor, R2, within the A5 Data Probe. Data/Cal Relay K2 allows the voltage to be read either across the unknown resistor, or the A5 Data Probe resistor in series with the unknown resistor. The voltages in the ohmmeter function are measured with both Q3 and Q4 off, selecting the 2.5V input range.

8-188. Resistance measurements are normally performed on passive components; i.e., components which have no voltage across them. If, however, the A5 Data Probe is placed across a voltage source while the 5005B is in ohms function, the Overvoltage Detection Circuitry, made up of U6 and Q5, automatically prevents the unit from being damaged. U6 is the overvoltage detector. The sense line connects the input of U6 (pins 3 and 6) through R24 (10K) to the 2.0V source. U6B triggers at the upper threshold (2.95V) and U6A triggers at the lower threshold (0.9V). The outputs (U6 pins 7 and 1) are wired-ORed, translated by Q5, and sent as an interrupt flag to the microprocessor, indicating overvoltage (OVOL). When an OVOL interrupt is received, the microprocessor responds by opening the Ohm Control Relay K1, and Data/Cal Relay K2, isolating the A5 Data Probe and the A2 DVM assembly from the source.

8-189. A3 MICROPROCESSOR AND DISPLAY DRIVE ASSEMBLY

8-190. The A3 Microprocessor Assembly monitors and directs the overall operation of the 5005B. The main functional blocks include the microprocessor, Power-Up Reset, 10 MHz Oscillator and Clock Generator, address and data buffers, ROM (Read Only Memory) with I/O, RAM Timer/Synchronizer and RAM (Random Access Memory) with I/O, Display Decoder Driver, and Keyboard Encoder.

8-191. All internal operations of the instrument are directed by the microprocessor system (or kernel). The kernel consists of the microprocessor, its associated address and data buffers and decoders, ROM and RAM. The kernel operates by interpreting and responding to control programs, consisting of 6K bytes of 8085 assembly code, permanently stored in ROM.

8-192. The ROM and RAM devices are accessed by the microprocessor by placing an address on the Data/Address bus and either writing to or reading from the addressed device. The microprocessor CE, $\overline{RD}$ and $\overline{WR}$ output control lines determine which device is enabled. The ROM and RAM devices also contain I/O ports. These are used to control and direct the flow of data, back and forth over the buses. The I/O ports are contained within the RAM and ROM memory devices, but function independently. The microprocessor $\overline{IO/M}$ output control line selects between the I/O and Memory sections of the devices.

8-193. Power-Up Reset

8-194. When the LINE switch is turned on, +5 volts is applied to the Power-Up Reset circuit and the microprocessor. The +5 volts is integrated by the Power-Up Reset circuit, consisting of CR2, R29, and C16, generating a slow rising level at pin 36 of U16. The rise of the level is slow enough to provide a RESET interrupt (logic LOW) to the microprocessor. The delay generated is approximately 0.1-second, determined by the time constant set by R29 and C16. The level then remains high until the LINE switch is turned off.

8-195. CR2 provides a discharge path for C16 when power is removed. The $\overline{RST\ IN}$ reset to the microprocessor immediately directs it to fetch a "restart vector" from a fixed location in the ROM. This reset vector tells the microprocessor where to find the first routine that it is to execute, which is the Power-Up Self Check routine. This self-check routine runs tests on major circuits, and momentarily lights all the front panel LEDS for an operator's visual check. After a predetermined time, the program instructs the microprocessor to branch to the Norm Signature Analysis mode program.

8-196. Display Decoder Driver

8-197. The Display Decoder Driver (U6) is a complete display interface, capable of receiving and storing eight 8-bit words of display data. U6 decodes the data, and drives the display devices (on A4) with its self-contained multiplexed scan circuitry. The data is continously scanned into the display until the microprocessor signals a change in data by pulling the MODE pin 9 LOW. Data is then read directly from the microprocessor DATA bus (lines A through H) and automatically sequenced into the U6 memory on successive negative going $\overline{WRITE}$ pulses.

8-198. Keyboard Encoder

8-199. The Keyboard Encoder (U3) is a CMOS, 16-key encoder, containing all the necessary logic to scan and encode the status of an array of SPST switches. Whenever a front panel key is pressed, DATA AVAILABLE (pin 13) goes HIGH. The next clock pulse causes a HIGH out on pin 5 of D-Flip-flop U5. This sends an interrupt (RST 6.5) to the microprocessor. The microprocessor responds by setting pin 3 of U9 low, activating the OUTPUT ENABLE for U3 and resetting interrupt flip-flop U5. The status of all the front panel switches is placed on the DATA bus via lines A through E. An internal register within U3 remembers the last key pressed. After the new switch status is stored by the microprocessor, the Keyboard Encoder returns to a monitor scan operation until another key is pressed. The DATA AVAILABLE line is also routed to the I/O of U4 (pin 31) to notify the microprocessor the keypress is being held. This allows the microprocessor to discriminate between a normal keypress and the use of the ADJUST/NOISE MARGIN keys, which step up or down as long as the key is held. C6 sets the frequency of the internal scan oscillator, and C7 compensates for key bounce.

8-200. 10 MHz Oscillator and Clock Generator

8-201. The 10 MHz Oscillator (U1) is the main timebase for the instrument. U1 is a hybrid three-terminal oscillator, which generates a 10 MHz square wave at approximately four volts p-p. The 10 MHz output from pin 8 of U1 is buffered by Q1, and routed through R19 and J1 pin $\overline{16}$ to the other

assemblies. R17 and Schottky diode CR1 insure Q1 remains biased ON. R1, C1, C2, and C3 filter the +5 volt supply to U1. The 10 MHz Oscillator output is also routed to the clock input (pin 11) of D-flip flop U5B. U5B is a divide-by-two Clock Generator, which produces the normal and complemented (via inverter U10) 5 MHz clocks for the microprocessor X1 and X2 inputs.

8-202. Microprocessor

8-203. The A3 Microprocessor Assembly uses the Intel 8085 microprocessor (U16). The microprocessor is the source of all major control of the 5005B. It is a fully contained processing unit that actively responds to the 5005B state and controls, and makes logic decisions. The microprocessor has 11 inputs, 19 outputs, and 8 multiplexed input/outputs.

8-204. Microprocessor Inputs

8-205. Seven of the 11 possible inputs are used. These are capable of halting the microprocessor. The inputs are described below.

8-206. X1 and X2. X1 and X2 are the clock inputs for the microprocessor. The true and complemented 5 MHz square waves from the divide-by-two Clock Generator are input to U16 on pins 1 and 2. These inputs provide all the timing and synchronization signals for the microprocessor system. An internal clock generator within U16 again divides X1 by two, producing a 2.5 MHz clock. This clock is also used within the microprocessor and output as CLK (pin 37), a control line to the microprocessor system.

8-207. $\overline{\text{RST IN}}$. The microprocessor $\overline{\text{RST IN}}$ input is generated by the Power-Up Reset circuitry. When power is applied to A3, an integrated dc level at U16 (pin 36) rises from ground (logic LOW) to +5 volts (logic HIGH), slowly enough to provide an active (LOW) reset interrupt to the microprocessor. This reset input directs the microprocessor to automatically fetch the restart vector from ROM, which properly references the microprocessor to the system program.

8-208. READY, RST 5.5, RST 6.5, and RST 7.5. These inputs are control signals used by the microprocessor. ROMs U4, U11, and U13 signal the microprocessor via the READY input. The reset inputs represent conditional interrupts: RST 5.5 indicates an overload or overvoltage state from the A2 DVM, RST 6.5 indicates a front panel key has been pressed, and RST 7.5 is a 250-microsecond interrupt, utilized during count modes to check for overflows.

8-209. Microprocessor Outputs

8-210. Fourteen of the 19 outputs from the microprocessor are used. The outputs are described below.

8-211. ADRS LINES. The 8085 microprocessor has 16 address lines, A0 through A15. The higher order lines, A8 through A13, are dedicated address control lines. A14 and A15 are not used. The lower order lines, A0 through A7, are combined with the Data bus lines, in a mutiplexed Address and Data Bus system. The Address lines of the microprocessor are used to logically address specific locations in the microprocessor address space. The functional blocks accessed by the address lines are: the Keyboard Encoder U3, the ROMs U4, U11, U13, the RAM/Timer U8, and various control circuit blocks. All reside at a specific address or block of addresses as viewed by the microprocessor.

8-212. The following memory and I/O maps, *Tables 8-4* and *8-5*, list the addresses and the addressed device, for the A3 Assembly. The H symbol in the address indicates a hexadecimal address.

Table 8-4. Memory Map

ADDRESS	ADDRESSED DEVICE
OH to 7FFH	ROM (U11)
800H to FFFH	ROM (U13)
1000H to 17FFH	ROM (U4)
3800H to 38FFH	RAM (U8)

Table 8-5. I/O Map

ADDRESS	ADDRESSED DEVICE
OH	ROM (U11) PORT A
1H	ROM (U11) PORT B
8H	ROM (U13) PORT A
9H	ROM (U13) PORT B
10H	ROM (U4) PORT A
11H	ROM (U4) PORT B
39H	RAM (U8) PORT A
3AH	RAM (U8) PORT B
3BH	RAM (U8) PORT C
8H input	Keyboard Controller
28H output	Display Controller
80H	Dummy I/O Port*

*Provides Start and Stop signals for another Signature Analyzer, for Diagnostic and Test purposes.

8-213. DATA LINES. The 8085 microprocessor utilizes a multiplexed Address and Data bus system. Lines AD0 through AD7 function as both lower order Address lines and Data lines. The Address/Data bus functions as an Address bus during the first half of the microprocessor cycle and as a Data bus during the second half of the cycle. The microprocessor is designed to logically separate the signals transmitted on this bus and to place data on the bus for use by the microprocessor. Address and Data information is placed on the bus structure in 8- or 16-bit parallel bytes.

8-214. CONTROL LINES. The remaining six microprocessor lines, ALE, RST OUT, CLK, IO/$\overline{M}$, $\overline{RD}$, and $\overline{WR}$, are output Control lines. They are used for the control and timing of the microprocessor system. ALE, Address Latch Enable, notifies the RAM and ROM devices when bus address information is valid, instructing them when to latch the data in. RST OUT is a Reset, used to initialize or reset the I/O sections of RAM and ROM. CLK, Clock, is a 2.5 MHz squarewave, used as a master clock for the RAM and ROM devices. IO/$\overline{M}$, I/O port/Memory, enables either the I/O port or Memory section of the RAM and ROM devices. The $\overline{RD}$, Read, and $\overline{WR}$, Write, lines are used to configure the RAM and ROM with I/O devices, to be read from, or written to the Address/Data bus.

8-215. Buffer Circuits

8-216. The bidirectional Buffer (U14) is used to buffer and isolate the microprocessor Address/Data bus lines. U14 is also used to implement the free-run function for Signature Analysis. The direction of data flow is determined by the $\overline{RD}$ line from the microprocessor, via inverter U7.

8-217. Address Decoder U15 is used to decode address lines A11, A12, and A13. This circuit generates the clock enables, CE, CE1, CE2, and CE3, for the RAM (U8) and ROMs (U11, U13, and U4). It also helps generate the $\overline{OUTPUT\ ENABLE}$ and $\overline{WRITE}$ for the Keyboard Encoder U3 and Display Decoder Driver U6.

8-218. ROM and I/O

8-219. The 5005B utilizes 5144 bytes of ROM, contained in three integrated circuits: U4, U11, and U13. The circuits are capable of decoding the multiplexed AD0-AD7 bus, utilizing the other control lines from the microprocessor. When addressed, the ROMs place the data contained in the addressed location on the Address/Data bus, in eight-bit parallel bytes, for use by the microprocessor.

8-220. Two 8-bit I/O ports are also contained within each integrated circuit. When the I/O portion of the integrated circuit is addressed, the I/O port can be written to or read from, depending on the previous programming. The I/O portion is programmed by writing to a specific location in the integrated circuit combined with certain conditions being met on the control lines. The IO/$\overline{M}$ line determines whether the I/O or the memory portion of the ROM is addressed.

8-221. RAM/Timer with I/O

8-222. U8 is the RAM/Timer with I/O. The RAM is addressed from memory location H3800 to H38FF. The Timer and I/O registers are addressed at defined I/O locations. The Timer is an essential element during frequency modes, used to generate the one-second gate. The 2.5 MHz CLK output from U16 (pin 37) is routed to TIMER IN of ROM/Timer U8 (pin 3). This clock drives an internal programmable counter, which generates a microprocessor interrupt every 250 microseconds. The interrupt is output on TIMER OUT (pin 6) which is routed as a RST 7.5 reset to the microprocessor. During frequency modes, an internal register within the microprocessor is preset to the number "4000". The register decrements with every RAM/Timer interrupt, while the microprocessor checks for overflows in the FSR. At the completion of "4000" 250-microsecond periods, (the one-second gate), the microprocessor turns off the GATE, and issues a series of control signals which turn off the Gate LED and change the configuration of the A1 Select Circuits.

8-223. Timer/Synchronizer

8-224. Timer/Synchronizer U12A is a D-flip-flop. U12A synchronizes the $\overline{\text{TIMER OUT}}$ signal from U8 (pin 6) to the CLK output of the microprocessor U16 (pin 37), to assure better accuracy.

8-225. A4 DISPLAY AND KEYBOARD ASSEMBLY

8-226. The A4 Display Assembly contains the six 7-segment LEDs used for the Display, the front panel keyboard, the Key Indicator LEDs, and some additional status display LEDs. The 12 additional status display LEDs are driven as follows: DS7, DS8, DS18, DS30-33 are driven by A3U2 and A3U4, and DS19-23 are driven by A8U1 and A8U6. All the remaining keys and LEDs are multiplexed, driven by buses from the A3 Microprocessor assembly.

8-227. Microprocessor A3U16 writes the characters and LED status information to the Display Decoder Driver A3U6. U6 properly sequences all strobes, segment lines, and LED drive lines, in a multiplexed configuration, before routing the display buses to the A4 Display Assembly via the A8 HP-IB Assembly. The main Data Display consists of five 7-segment LEDs, DS1 through DS5, and the polarity sign indicator DS6. Data for the Display is decoded on A3, and placed on the Display Data bus lines, "a through g, and dp", one digit at a time. As each digit's data is placed on the bus, the appropriate control line, DEVICE ENABLE 0 through 5, enables the corresponding seven-segment LED. The DEVICE ENABLE lines continuously cycle, strobing data into the Display LEDs. The Key LEDs and Status LEDs are configured into a matrix, selected and strobed by the same Display Data bus lines and DEVICE ENABLE 6 and 7.

8-228. The A4 Keyboard, consisting of 21 momentary-closure pushbutton switches, S1 through S21, is also configured into a matrix. The status of switches S1-11 and S13-20 is continuously monitored by nine lines, X1 through X4 and Y1 through Y5, from the A3 Keyboard Encoder. A3U3 detects when any key is pressed and generates an interrupt which is sent to the A3 microprocessor. The microprocessor responds by reading the Keyboard Encoder memory and resetting the Keyboard Encoder interrupt flip-flop A3U5. Switches S12 and S21 are monitored by lines X5 and Y6-7 from the A8 Keyboard Eencoder (U20). A8U20 detects the keypress and interrupts the A8 microprocessor (U7), resetting the Keyboard Encoder interrupt flip-flop A8U21.

8-229. A5 DATA PROBE ASSEMBLY

8-230. The A5 Data Probe contains the 10:1 Passive Divider, Reference Resistor, Probe Switch, and Logic State Indicator lamp. Analog and digital data signals are input to the HP 5005B through the probe tip of the A5 Data Probe. The signals are attenuated by a factor of 10 by the passive divider network consisting of R1, C1, in conjunction with A1R7 and A1R8. A5R2 is the 20K ohm Reference Resistor, used during the Ohmmeter function. DS1 is the probe Logic State Indicator, an incandescent lamp driven by the Data Probe Light Driver circuit on A1. A5S1 is a momentary switch used in REMOTE mode to allow operator interaction with a controlling device for data input. In LOCAL, it is used in the ΔV mode. There are no active components on A5.

8-231. A6 TIMING POD ASSEMBLY

8-232. A6 Timing Pod receives the three major timing signals for the HP 5005B: START/ST/SP, STOP/QUAL, and CLOCK. Each of the three signals passes through the first stage of its own passive divider network. The remaining components for the final stage of each divider are located on A1. The signals are attenuated by a factor of 10 as they are routed to the Input Voltage Comparators on A1. There are no active components on A6.

8-233. A7 LINE MODULE ASSEMBLY

8-234. The A7 Line Module Assembly is attached to the rear of the A1 Main Assembly. It contains the connector for the power cable, the line fuse, line input filtering cooling fan, and a printed-circuit card. The printed-circuit card can be inserted in any one of four positions to select 100-, 120-, 200-, or 240-volt ac operation. The schematic for the A7 Line Module Assembly is shown in *Figure 8-19*. A detailed description, including instructions for changing the fuse or voltage selection is given in paragraph 2-8.

8-235. A8 HP-IB/A9 INTERFACE ASSEMBLIES

8-236. The HP-IB interface assembly is made up of five major blocks. These blocks are the microprocessor control circuitry, the interface to the display and keyboard, the HP-IB interface, the circuitry for controlling the 5005B unique keys and display, and diagnostics.

8-237. Microprocessor Control Circuitry

8-238. The microprocessor circuitry (kernel) on the A8 board controls the interface to the display and keyboard as well as HP-IB operation. The kernel functional blocks include the 8085 microprocessor, power-up reset, crystal oscillator, address latch for lower order address bits, address decoder, RAM and ROM.

8-239. The power-up reset (C13, R27, and CR5) provides a 100 ms reset pulse to the microprocessor when power is applied or interrupted. This reset pulse directs the microprocessor to a known memory location to fetch the first instruction to be executed.

8-240. The crystal oscillator circuitry (U1, C11, C12) provides a fixed 4 MHz clock signal to the microprocessor. This clock is the timebase for all operations on the A8 HP-IB assembly.

8-241. The 8085 microprocessor uses a multiplexed address/data bus. The eight lower order address bits appear on the bus during the first clock cycle and must be latched for stable addressing of memory and I/O devices. The falling edge of the Address Latch Enable (ALE) control line from the microprocessor is used to latch the address information (A8U22).

8-242. The address decoders (A8U15 and U21) and the microprocessor control lines $\overline{RD}$ and $\overline{WR}$ implement memory mapped I/O for the A8 board microprocessor. Memory and I/O devices are enabled when the processor does a read or write to the appropriate device address. See memory map shown in *Figure 8-10*. The memory portion of the kernel is composed of 8K bytes of Read Only Memory (A8U23) and 1K byte of Random Access Memory (A8U24).

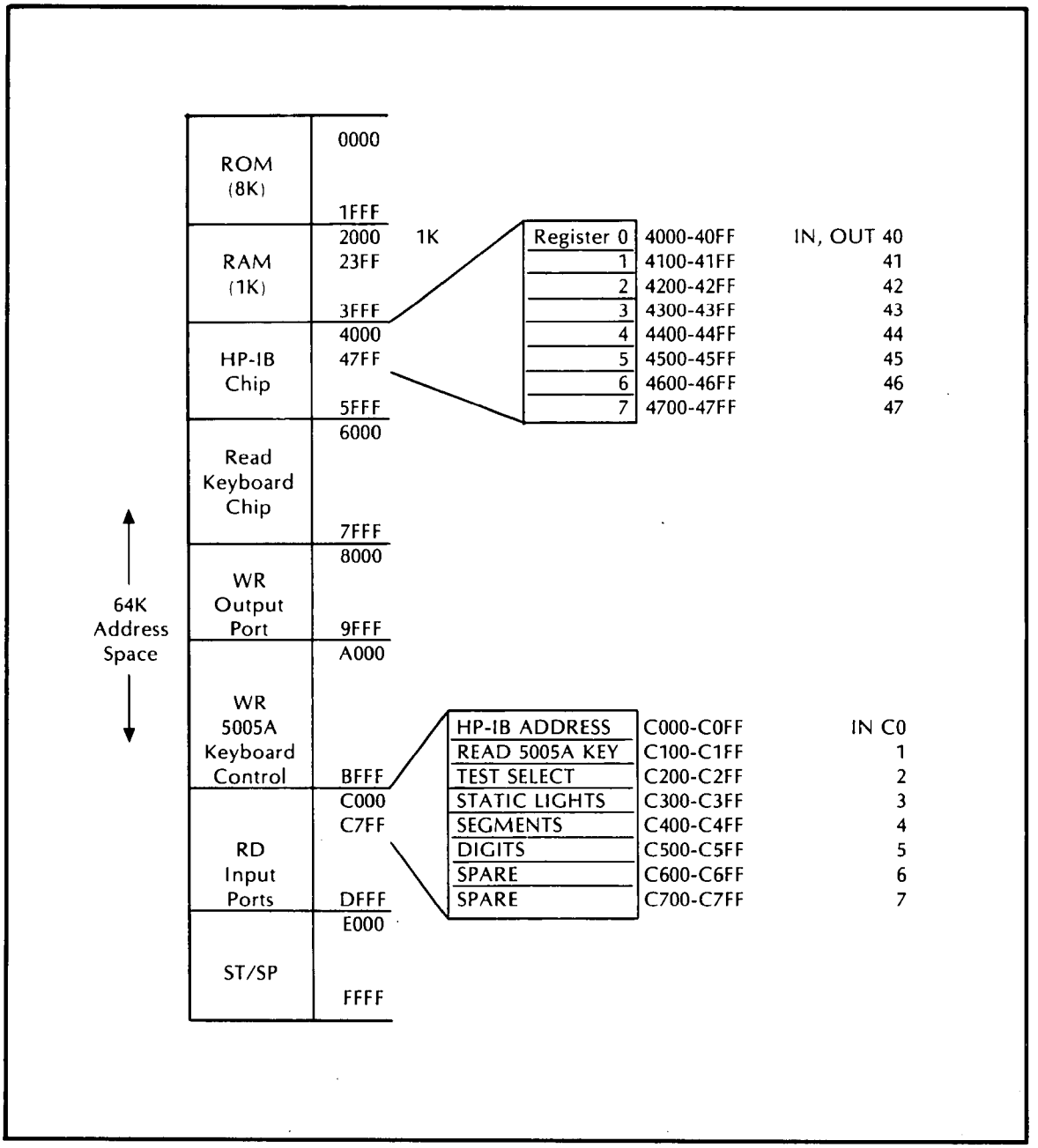


Figure 8-10. A8 HP-IB Memory Map

8-243. Interface to the Display and Keyboard

8-244. The display and keyboard information from the A3 Microprocessor Assembly is routed to the A8 HP-IB Assembly. This allows the HP-IB processor to monitor the display and control the keyboard.

8-245. The display is generated by an Intersil 7218 display driver chip (A3U6). The data is multiplexed in the form of 8 digits, each with 8 bits of segment information. The HP-IB processor has an 8-bit input port tied to the 8-digit lines (A8U12) and an 8-bit input port tied to the 8 segment lines (A8U13). To read the display data, the HP-IB processor waits for each successive digit line to become active, then latches the segment information for each digit. The segment information is then decoded by the HP-IB processor and stored for later use. To guarantee proper dc drive levels for the segment and digit input ports, the segment lines are buffered by ICs U2 and U3.

8-246. There are seven additional bits of nonmultiplexed display information that are driven directly by output ports on the A3 board. These bits are buffered on the A8 board (A8U4) and are also connected to a HP-IB input port (A8U14). This allows the HP-IB processor to input data from these seven bits.

8-247. The keys on the 5005B front panel must be remotely controllable through HP-IB (with front panel keys disabled) and must also function in the local mode. The keyboard portion monitored by A3 is implemented by a National 74C923 key encoder. This IC allows for a 4 by 5 matrix of keys, and has built-in scan circuitry and debounce. The key encoder works as follows (refer to *Figure 8-11*).

> Assume the key located at the intersection of the second row and the fifth column is depressed. The key encoder asserts each row sequentially and watches for one of the five columns to be asserted. In our example, the second row will be asserted by the key encoder. When the key encloder looks at the column lines, it will see that the fifth column line is asserted. The encloder generates an interrupt to the A3 processor and reports a key push.

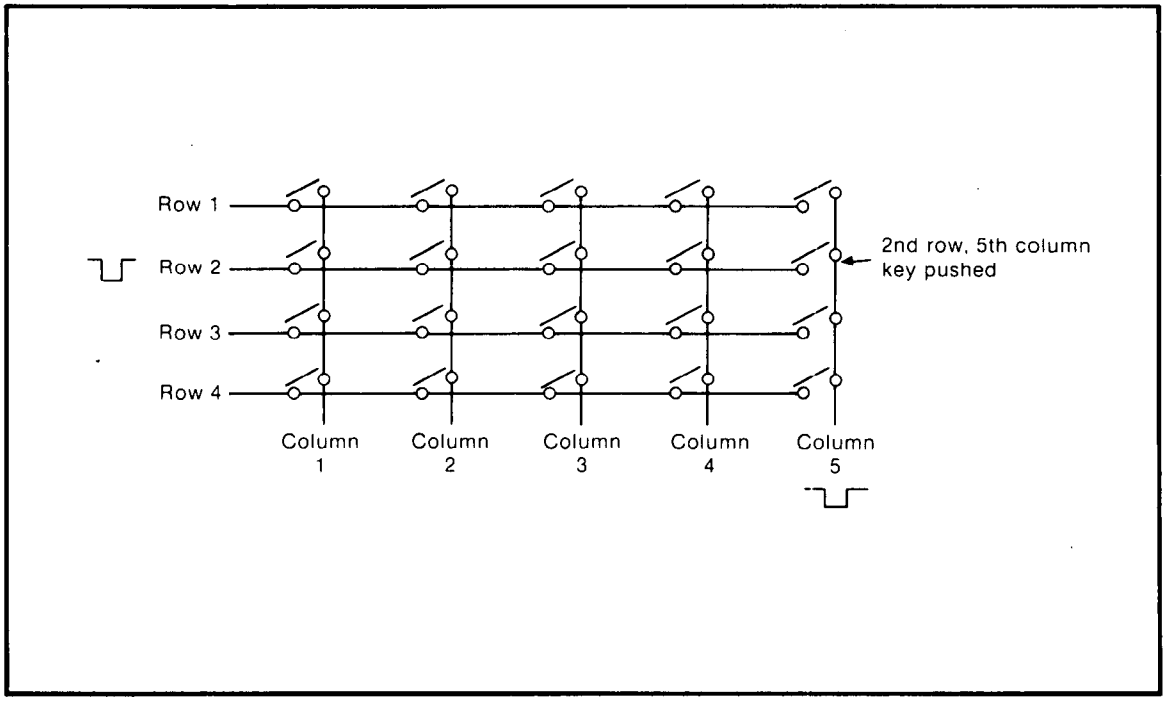


Figure 8-11. A8 HP-IB Key Matrix

8-248. The HP-IB processor simulates the key push in REMOTE mode by use of an input port A8 (½ U18) attached to the row lines and an output port (A8U11) attached to the column lines. The HP-IB processor can push the same key as in the previous example as follows:

> The input port monitors the row lines until it sees the second row line asserted. The output port then drives the fifth column line to its active state. The key encoder chip knows its second is asserted and see the fifth column active. Again, it interrupts the A3 processor to report a key push.

8-249. The front panel keys must be deactivated when the 5005B is remotely controlled by the HP-IB. This is accomplished by a three-state buffer (A8U19). The buffer is inserted in the 5 column lines after the front panel keyboard. In REMOTE operation the buffer is disabled so any activity on the keys is prevented from reaching the column inputs of the key encoder chip. In local operation the buffer is enabled. When a front panel key is pushed, the appropriate column line is activated and the A3 processor seees the key push. Diodes CR1-CR4 in the row driver lines prevent the key encoder row drivers from being shorted together when more than one key is pused.

8-250. A3 HP-IB Interface Circuitry

8-251. The HP-IB interface to the 5005B is implemented with an HP-IB chip, the 8291A (A8U9), which serves as the interface between the 8085 microprocessor and HP-IB. All the interface functions defined in the IEEE-488 Standard are implemented in the 8291. Its capabilities include: data transfer, handshake protocol, talker/listener addressing procedures, device clearing, triggering, and service requests. HP-IB interface block consists of the HP-IB chip, bus transceivers, and HP-IB address select circutiry.

8-252. The 8291 architecture includes eight registers that may be written into by the processor and another eight registers that can be read by the processor. One read and one write register are dedicated to direct data transfer. The rest of the write registers control the operating features of the chip. The read registers allow the processor to monitor various bus conditions and device conditions.

8-253. The 8291 chip is connected to HP-IB through noninverted transceivers, which provide the DC drive levels and isolation required by the IEEE-488 standard. Two 8-bit transceivers are used: one for the HP-IB control lines (A8U17) and the other for the 8-data lines (A8U10). The T/$\overline{R1}$ control line from the 8291 chip determines whether the transceivers are transmitting information over the bus or receiving information from the bus.

8-254. The HP-IB talker/listener address select switch is located on the A9 Assembly. The switch is connected to an input port (A8U25) of the microprocessor. On power-up of the 5005B, the processor reads this port to determine the talker/listener address. The input port is protected from static discharge by diode pack CR6.

8-255. Unique Keys and Display

8-256. The 5005B has five LEDs, three keys and an HP-IB controllable beeper that are unique to the A8 HP-IB Assembly. The five LEDs are controlled by a processor output port (A8U16). The port outputs are buffered (A8U6) to provide sufficient LED drive current. The unique keys, two on the front panel and one located on the data probe, are monitored by the same type key encoder chip (A8U20) used in the A3 assembly. This encoder scans the keys and interrupts the HP-IB processor when a key is pushed.

8-257. The alarm is controlled by the same output port that controls the LEDs (A8U16). A software-generated 2 kHz square wave produces the alarm tone. The 2 kHz signal from the port

drives a buffer (A8U1) which drives a transistor (A8Q1) operating as a saturated switch. The transistor is connected to the alarm through a resistor that sets the beeper volume. Two bits of the output port are used to provide two volume levels.

8-258. Diagnostics

8-259. The diagnostic circuitry consists of a switch connected to the HP-IB processor input port A8 (½ U18). The port is read during the microprocessor power-up routined. If the switch is set to something other than the normal operating position, the HP-IB microprocessor will run the selected diagnostic test.

8-260. The HP-IB microprocessor can be placed in the freerun mode by removing jumper pack W1-W9 and cycling the line power. When the jumpers are removed, the microprocessor is isolated from the rest of the data bus. The power-on reset cycle causes the microprocessor to place the address of the first instruction to be executed on the multiplexed address/data bus. The lower 8 bits of this address are latched by U22. The microprocessor then three-states the address/data bus and initiates a read cycle to read the first instrument from memory. When the RD control line becomes active U1 forces the AD7 bit low. The other 7 bits of the data bus are forced high by resistor pack R37. Thus, when the microprocessor reads the first instruction, it sees AD0 through AD6 high and AD7 low. This bit pattern corresponds to the instruction MOV A,A, which is essentially a no-operation (NOP) instruction. The microprocessor then increments its program counter and reads the next instruction in the same way. Each instruction read by the micrprocessor is a NOP, so the microprocessor continually steps through its entire address space.

8-261. During the time that the address is present on the multiplexed bus, the RD control line is high. This places the output of U1 (pin 10) in the high impedance state and the AD7 line is unaffected. When the shorting bars are in place, the output of U1 is always in the high impedance state and normal operation is not affected.

8-262. TROUBLESHOOTING

8-263. Introduction

8-264. The HP 5005B is a microprocessor-based system. The majority of the instrument circuitry consists of digital logic configurations. The primary method of fault location is through signature analysis, keyed to built-in Diagnostic routines.

8-265. The digital voltmeter, power supply, and much of the input circuitry including Data Probe, Timing Pod, comparators, and DACs are analog circuit configurations. These circuits are supported with more conventional troubleshooting techniques, including built-in Diagnostic routines as well as active signal tracing.

8-266. Troubleshooting information is provided through various troubleshooting procedures, described in this section. Diagnostic troubleshooting information is also provided in abbreviated form on corresponding assembly Service Sheets.

8-267. Troubleshooting Flowchart

8-268. The basic troubleshooting technique is illustrated in the Overall Troubleshooting Flowchart, *Figure 8-12*. No troubleshooting system or philosophy is failsafe. This flowchart attempts to show how best to interpret the indications provided by the Power-Up Self Check, Error Messages, and Display to initially isolate the trouble. Individual troubleshooting procedures are provided for the Power Supply, Kernel, and Assemblies A1, A2, A3, and A4. The A8/A9 HP-IB Assembly/Interface is tested individually as described in paragraph 4-24. The Overall Troubleshooting Flowchart should help direct the technician to the proper procedure. The use of the

flowchart is described in Overall Troubleshooting, beginning with paragraph 8-281. Once familiar with the individual Diagnostic Procedures, the technician may proceed directly to indicated assembly Service Sheets for specific troubleshooting information and abbreviated Diagnostic Procedures.

8-269. Troubleshooting Aids

8-270. The 5005B provides a variety of built-in troubleshooting aids, within the firmware of the instrument. These include an initial Power-Up Self Check routine with corresponding Error Messages, and a series of user-designated Diagnostics. These aids are explained in detail in the following paragraphs, and in abbreviated form on associated Service Sheets. A thorough understanding and use of these aids will greatly assist the technician in the location of faults.

8-271. Power-Up Self Check

8-272. The HP 5005B, upon power-up, performs a series of self-tests which exercise a sampling of internal circuitry. Detected circuit failures or calibration errors may result in the display of a ERR 15 message. **If this error message occurs, refer to to paragraph 3-94 for further error identification procedures.** Although the power-up test is not a 100% validation of the circuit performance, it does provide a fast, convenient method of establishing a level of confidence. Successful completion of the Power-Up Self Check is indicated by a display of four bars (————), with the instrument in the NORM Signature Analysis mode. Refer to paragraph 3-32.

8-273. To identify errors 0-20, the error trap routine described in Paragraph 3-94 must first generate an error 49. This indicates that a hardware error in the "5005A" portion of the 5005B has been detected. At this point, it is necessary to configure the 5005B as a "5005A". The procedure is described below.

8-274. Configuring the 5005B as a 5005A

8-275. To check for errors 0-20, do the following:

a. Disconnect the 5005B from ac power.

b. Remove the top cover and top strut as described in Paragraphs 8-66a and c.

c. Disconnect and remove the A8 HP-IB Assembly as described in Paragraph 8-82.

d. Reconnect the A4 Front Panel Assembly to the A3 Microprocessor Assembly with the 50-pin grey ribbon cable (A4W1) leading from the Front Panel Assembly. The connector and the A3 Assembly are keyed to ensure proper positioning of the edge connector pins. Note that the edge donnector of the A3 Assembly has only 34 pins.

e. Reconnect ac power to the instrument and turn on the power switch.

f. The display should now indicate an error message from 0 to 20.

g. Refer to *Table 8-6* for a description of these errors.

Table 8-6. Error Messages

ERROR	DESCRIPTION	ASSOCIATED ASSEMBLY
	5005A ERRORS	
Err00	ROM checksum error	A3
Err 01-03	Not Assigned	
Err04	RAM read/write error	A3
Err05	Not Assigned	
Err06	Timer error	A3
Err07	DVM/Ohmmeter Zero Offset exceeds ±-00200	A2
Err08	DVM data exceeds 32000	A2
Err09	DVM 10V calibration measurement on 25V range exceeds 10.3V	A2
Err10	DVM 10V calibration measurement on 25V range is less than 9.3V	A2
Err11	DVM 10V calibration measurement on 250V range exceeds 10.3V	A2
Err12	DVM 10V calibration measurement on 250V range is less than 9.3V	A2
Err13	OHMS 2V calibration exceeds 2.1V	A2
Err14	OHMS 2V calibration is less than 1.9V	A2
Err15	Internal count test or keyboard error	A1
Err16	DAC Zero Offset exceeds 200 mV	A1
Err18	DVM measurement timeout: M/Z status incorrect	A1/A2
Err19	DVM data transfer error: digit strobe status incorrect	A1/A2
Err20	Keyboard error: Keyboard encoder DATA VALID signal error	A1/A4
	5005B ERRORS	
Err40	Function key LED error	A4
Err41	Attempt to push illegal keycode (>18)	A4
Err42	Unrecognized character read from the display	A4
Err43	No response to key depression	A4
Err44	Internal error during command parsing	A8
Err45	Internal error	A8
Err46	Invalid interrupt on HP-IB Interrupt	A8
Err47	Illegal keycode read from A8 Keyboard Encoder	A8
Err48	7218 Display chip digit strobe error	A8
Err49	ErrXX read from "5005A" display	N/A
Err50	2 or more mutually exclusive LEDs ON during "SU" execution	A4
Err81	Command string too long	N/A
Err82	No match for HP-IB command	N/A
Err83	Illegal or missing numeric trailer in HP-IB command	N/A
Err84	Attempted edge or threshold select not active in function	N/A
Err85	8291 HP-IB chip "Err" bit set	N/A
Err86	Illegal threshold voltage command format	N/A
Err87	Programmed threshold voltage out of range	N/A
Err88	Delta Volts reference no longer valid	N/A

8-276. The power-up self test performed by the instrument in "5005A" mode can be divided into seven subsections. They are:

- ROM test
- RAM test
- Timer test
- DVM test
- Partial DAC test
- Internal Count test
- LED test

a. ROM Test

Associated Error Messages: Err00 ROM checksum error.

The ROM test does an arithmetic computation which uses all the words stored in Read Only Memory as addends. The microprocessor computes an arithmetic sum and compares this sum to a previously computed (by the designer) sum stored in ROM. If the two results are not equal the 5005B attempts to display Err00.

b. RAM Test

Associated Error Messages: Err04 RAM read/write error.

The RAM test writes the low order address byte of the addressed byte into the addressed byte (address as data). This is performed on all 256 RAM locations. The 256 locations are then read from and the contents are compared to the original data stored there. The complement of the original data is then stored in each location and read for comparison. If either test fails (i.e., the read byte does not equal the written byte), the 5005B attempts to display Err04.

c. Timer Test

Associated Error Messages: Err06 Timer error.

The Timer test exercises the timer and its associated flip-flop and microprocessor interrupt. A gross comparison of timer accuracy to the cycle time of the microprocessor is performed. If either circuit fails the 5005B attempts to display Err06.

d. DVM Test

Associated Error Messages:

Err07 DVM or Ohmmeter Zero Offset exceeds ±00200.
Err08 DVM data exceeds 32000.
Err09 DVM 10V calibration measurement on 25V range exceeds 10.3V.
Err10 DVM 10V calibration measurement on 25V range is less than 9.3V.
Err11 DVM 10V calibration measurement on 250V range exceeds 10.3V.
Err12 DVM 10V calibration measurement on 250V range is less than 9.3V.
Err13 OHMS 2V calibration exceeds 2.1V.
Err14 OHMS 2V calibration is less than 1.9V.
Err18 DVM measurement timeout (M/Z status incorrect).
Err19 DVM data transfer error (digit strobe status incorrect).

The DVM test performs many measurements. The first is a test of the functions associated with the DVM IC's U4 and U7, including the Zero Offset. If the results fall outside a preset range the 5005B attempts to display Err07. If the accumulated data exceeds 32000 counts, the 5005B will attempt to display Err08.

If Zero Offset passes, the 5005B attempts an auto calibration routine. If the calibration voltage (nominally 10.0V) falls outside a preset limit (as described in Err09-Err12), the 5005B attempts to display the appropriate message.

The 2.0 Volt reference associated with the Ohmmeter circuitry is checked next. If it falls out of a preset range (described in Err13 and Err14) the 5005B attempts to display Err13 or Err14.

The 5005B will attempt to display Err18 if the M/Z status bit of U7 (on the DVM board) does not go low to indicate a data transfer within the proper time frame. The 5005B will attempt to display Err19 if a strobe pulse does not occur within the proper time frame.

e. Partial DAC Test

Associated Error Messages: Err16 DAC Zero Offset exceeded 200 mV.

This test checks two of the four DAC's on the Main Assembly. DACs U1 and U4 are addressed and tested. If either output exceeds 200 mV, the 5005B attempts to display Err16.

f. Internal Count Test or Keyboard Error

Associated Error Messages: Err15 Internal Count Test.

During this test, the internal 10 MHz clock is routed to the internal counter and a check is made of the counter circuits. Much of the Signature Analysis circuitry is verified by this

test. If the normal output from this test is not found, the 5005B attempts to display Err15. If a nonvalid code is received, the 5005B attempts to display Err15.

g. LED Test

Associated Error Messages: None

The LED test lights all the front panel LEDs, digit segments, and decimal points, except "GATE" and "UNSTABLE". The GATE and UNSTABLE LEDs should flash on momentarily during the cycle and therefore can be checked for operation. The operator must verify that all of the LEDs are functioning properly. An unlighted LED or LED segment indicates a bad device.

8-277. The HP-IB related errors can be divided into two subsections. They are:

- Hardware and Software related errors
- HP-IB command and Operation related errors

a. Hardware and Software related errors.

Associated error messages: Err40 through Err49.

These errors indicate a hardware or operating software related error. Service is needed to correct these errors. Err49 indicates additional testing to determine the "5005A" error that occured.

Err40: Function key LED error. Either none or more than one funbction key LED(s) on. Implies "5005A" failure, port C4 failure, or 5005B in some diagnostic mode, e.g., display test.

Err41: Attempt to push illegal key (>18). The HP-IB controller has sent a number greater than 18 in the command string to cause a keypush.

Err42: Unrecognized character read from display. Error was found during ASCII conversion. Possible "5005A" or Port C4 failure.

Err43: No response to key depression. Expected output of key response was not detected by the listening device.

Err44: Internal error during command parsing. Offset counter is incorrect. Fatal error.

Err45: Internal error. Parameter out of range.

Err46: Invalid interrupt on HP-IB interrupt line.

Err47: Illegal key code read from 74C923 KBD chip (A8U20).

Err48: 7218 Display chip digit strobe error. Implies 7218 (A3U6) failure or Port C5 failure.

Err49: ErrXX read from "5005A" display. Perform tests as indicated in Paragraph 8-274.

Err50: Two or more mutually exclusive polarity select LEDs, or polarity select LEDs found ON during "SU" execution.

b. HP-IB command and operation related errors.

Associated error messages: Err81 through Err88.

These errors indicate that the format or protocol of HP-IB commands was not followed in the data that was sent by the controller, or that the transmitted key strokes were not interpretable.

Err81: Command string too long (over 250 characters).

Err82: No match for HP-IB command. Implies illegal or incomplete HP-IB command.

Err83: Illegal or missing numeric trailer on HP-IB command.

Err84: Attempted selection of an edge select or threshold select not active in this function.

Err85: 8291 HP-IB chip "Err" bit set. Implies no active listeners on the bus. Controller error.

Err86: Illegal threshold voltage command format.

Err87: Programmed threshold voltage out of range.

Err88: Local key pushed and some function other than delta volts selected after remote selection of delta volts. The delta volts reference is no longer valid, resulting in the possibility of erroneous data being sent to the controller.

8-278. Built-in Diagnostics

8-279. The 5005B provides 28 user-activated Diagnostic troubleshooting routines, selectable through the two rotary switches (S1 and S2) on the A3 Microprocessor Assembly. All tests are initiated by setting the rotary switches to the appropriate switch codes and then turning the LINE switch to OFF and back to ON. A new test may not be initiated except by this power-down/power-up sequence. *Table 8-7* lists the test switch codes and explains each test.

Table 8-7. Diagnostic Switch Codes

SWITCH CODE		TEST DESCRIPTION	ASSOCIATED ASSEMBLY
SW1	SW2		
0	0	Normal operation.	
0	1	ROM diagnostic, SA compatible.	KERNEL/A3
0	2	Not assigned.	
0	3	RAM diagnostic, SA compatible.	A3
0	4	I/O diagnostic, SA compatible.	A3
0	5	Timer test.	A3
0	6	Signature analysis circuit diagnostic, SA compatible.	A1
0	7	Count diagnostic, SA compatible.	A1
0	8	Time interval diagnostic, SA compatible.	A1
***** Tests 09 to 0C test the DAC voltage levels referenced to the 5005B inputs. *****			
		DAC U1 DAC U4 DAC U7 DAC U13	
0	9	0.0V +7.65V 0.45V -7.65V	A1
0	A	-7.65V 0.0V +7.65V 0.45V	A1
0	B	0.45V -7.65V 0.0V +7.65V	A1
0	C	+7.65V 0.45V -7.65V 0.0V	A1
0	D	DAC ramp exercise: Programs all DACs to cycle from -12.75V to +12.75V in a repetitive ramp function.	A1
0	E	Display the V_P+ Zero Offset value.	A1
0	F	Display the V_P- Zero Offset value.	A1
1	0	Display the DVM Zero Offset value for the 25V range.	A2
1	1	Display the DVM AUTO-CAL value for the 25V range.	A2
1	2	Display the uncorrected DVM reading for the 25V range.	A2
1	3	Display the DVM Zero Offset value for the 250V range.	A2
1	4	Display the DVM AUTO-CAL value for the 250V range.	A2
1	5	Display the uncorrected DVM reading for the 250V range.	A2
1	6	Display the Zero Offset value for OHMS.	A2
1	7	Display the reference voltage for OHMS.	A2
1	8	Display the measured voltage for OHMS.	A2
1	9	Turn on all LEDs and display segments, and flash the "GATE" and "UNSTABLE" LEDs.	A4
1	A	Display a shifting pattern of all characters normally displayed.	A4
1	B	Display the "key code" of the last key depressed.	A4
2	(X)	Freerun: Force an aborted read of all memory content.	KERNEL

(X = don't care)

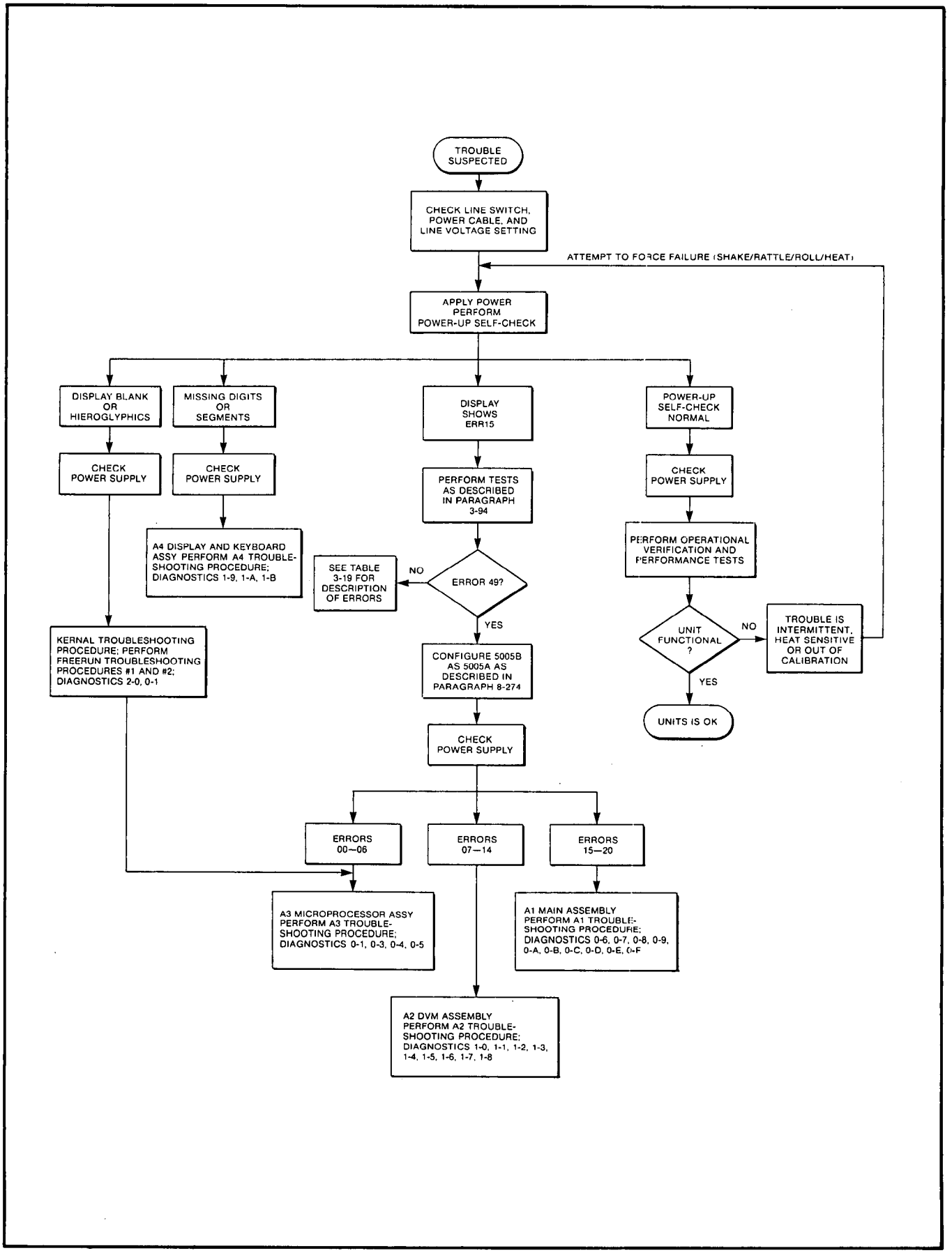


Figure 8-12. Overall Troubleshooting Flowchart

8-280. It should be noted that the majority of these tests are intended to be used only after the operation of the kernel has been sucessfully verified. The initial power-up self check will tell much about the status of the kernel. Referring to the Overall Troubleshooting Flowchart, any power-up indication, with the exception of Blank/Hieroglyphics or Error Message 00, generally indicates the kernel is functioning properly. Such symptoms allow the technician to logically bypass the extensive kernel Diagnostics, and proceed to a suspect assembly, where the local Diagnostic Procedures can be performed.

8-281. OVERALL TROUBLESHOOTING

8-282. All troubleshooting initiates with the Power-Up Self Check. In general, the Power-Up Self Check will produce one of four types of display: a blank or hieroglyphic display, a numbered Error message, a display with missing digits or segments, or a normal indication (four bars). The Overall Troubleshooting Flowchart illustrates the potential fault areas associated with each type of display. The technician should follow the flowchart procedure to identify the faulty assembly. Once the faulty assembly is isolated, the technician can proceed directly to the corresponding Service Sheet. The Service Sheet contains the schematic diagram, block diagram, component locator, associated Error messages, and abbreviated Diagnostic procedures.

8-283. The following procedure describes the recommended preliminary troubleshooting, and references the Overall Troubleshooting Flowchart in *Figure 8-12.*

a. Insure that the line voltage programming card is properly inserted for the intended line voltage. This card is located beneath the line fuse in the A7 Line Module. Hold the card so that proper voltage range can be read normally and place the top of the card first into the instrument. See *Figure 8-17.*

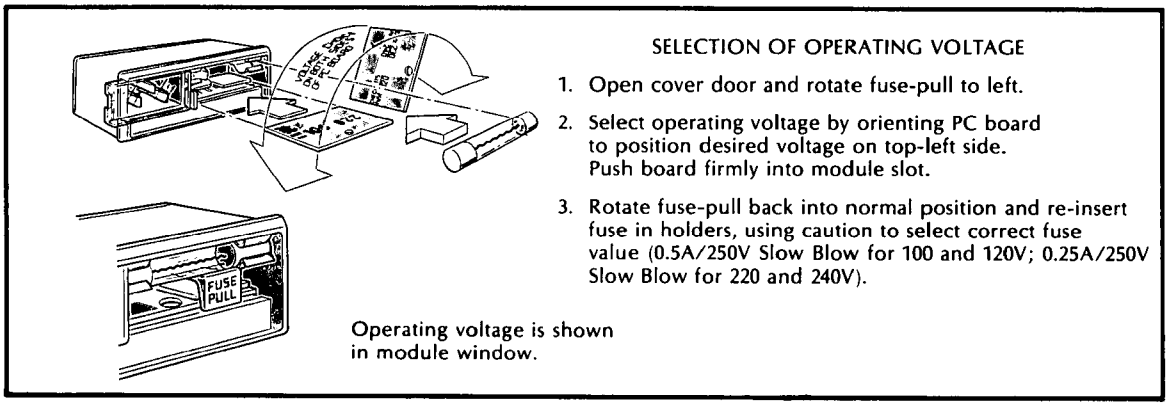


Figure 8-13. Line Voltage Selection

b. Connect the main power cable to the 5005B. Set the LINE switch to the ON position.

c. Observe the Display. The 5005B should immediately perform the Power-Up Self Check, (see paragraph 8-271), terminating in the NORM Signature analysis Mode. If a trouble exists, the operator should observe one of the following display responses:

1. Display Blank or Hieroglyphics. The display presents meaningless hieroglyphics or random segments, or no display at all.
2. Display Shows Error Messages. The display provides a numbered Error Message.
3. Missing Digits or Segments. One or more digits or segments in a digit do not light, but a legible non-intermittent display is visible.
4. Power-Up Self Check Normal. The power-up routine (see paragraph 3-32) appears normal. The instrument displays four bars (————) and assumes the NORM Signature Analysi mode.

d. For all failure indications, it is always recommended that the instrument's internal power supplies be checked first. The 5005B power supply contains four dc supplies: +5 volts, -5.2 volts, +12 volts, and -12 volts. These supplies are generated on the A1 Main Assembly, and are labeled in several locations. Measure each supply. If any supply appears low or high, refer to Power Supply Troubleshooting, Paragraph 8-284.

e. Display response (1.) indicates the trouble may be associated with the kernel. Perform the Kernel Troubleshooting Procedure, paragraph 8-292.

f. Display response (2.) is an indication that the kernel is functioning properly and that, in general, only the circuitry associated with the indicated error message need be checked. Refer to the Overall Troubleshooting Flowchart, *Figure 8-12*, for specific assembly procedures.

g. The probable cause of display response (3.) is an isolated faulty LED digit, or the associated digit driver circuit.

h. Display response (4.) could indicate the unit is operating properly and there is no trouble. It could also indicate an intermittent, heat sensitive, or calibration failure. Confirm by performing the Operation Verification and/or Performance Tests, and then attempt to force the suspect failure appear.

WARNING

ALL TROUBLESHOOTING PROCEDURES REQUIRE INTERNAL ACCESS TO THE INSTRUMENT WITH THE PROTECTIVE COVERS REMOVED. THESE PROCEDURES SHOULD BE PERFORMED ONLY BY TRAINED SERVICE PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED.

NOTE

To access the internal circuitry for the Timing Pod, Data Probe, or Main Instrument, refer to the Disassembly Procedures in paragraph 8-62.

8-284. POWER SUPPLY TROUBLESHOOTING

8-285. Remove the top cover and top strut of the instrument. If necessary, refer to the Disassembly and Reassembly procedures beginning with paragraph 8-62. Connect the main power cable, and set the LINE switch to ON. After the Power-Up Self Check routine is completed, measure the four dc voltages on the A1 Main Assembly using a digital voltmeter. The measurement locations are indicated in *Figure 8-14*. Verify that the measured voltages are within the tolerances listed below. If any supply is incorrect, review the following paragraphs. The proper voltages appearing at the power supply outputs are:

+5 volts dc ± or -0.25 volts
+12 volts dc ± or -0.6 volts
-12 volts dc ± or -0.6 volts
-5.2 volts dc ± or -0.26 volts

8-286. Referring to the schematic diagram in *Figure 8-15*, the positive dc supplies, +5V and +12V, derive their input from bridge rectifier CR6. The negative dc supplies, -5.2V and -12V, derive their input from bridge rectifier CR5. The output from the positive rectifier is protected by a 3-amp fast-blow fuse, F1. If the positive supplies are dead, check this fuse and replace if necessary, with HP Part #2110-0003. The main line fuse, within A7, is a half-amp slow-blow, HP Part #2110-0202, for the 100 volt settings, or a one-quarter-amp slow-blow, HP Part #2110-0201, for the 200 volt settings. Measure the output from the rectifiers with an oscilloscope, and compare the waveforms to *Figure 8-16*.

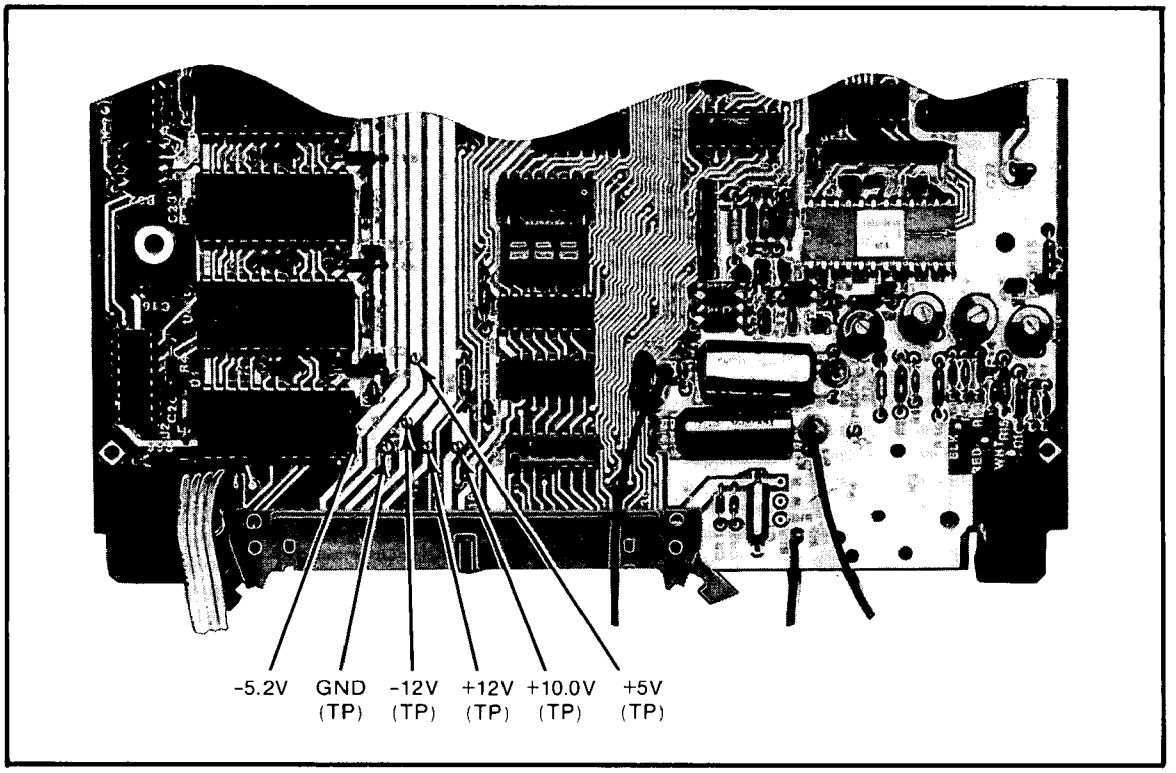


Figure 8-14. Power Supply Measurement Locations

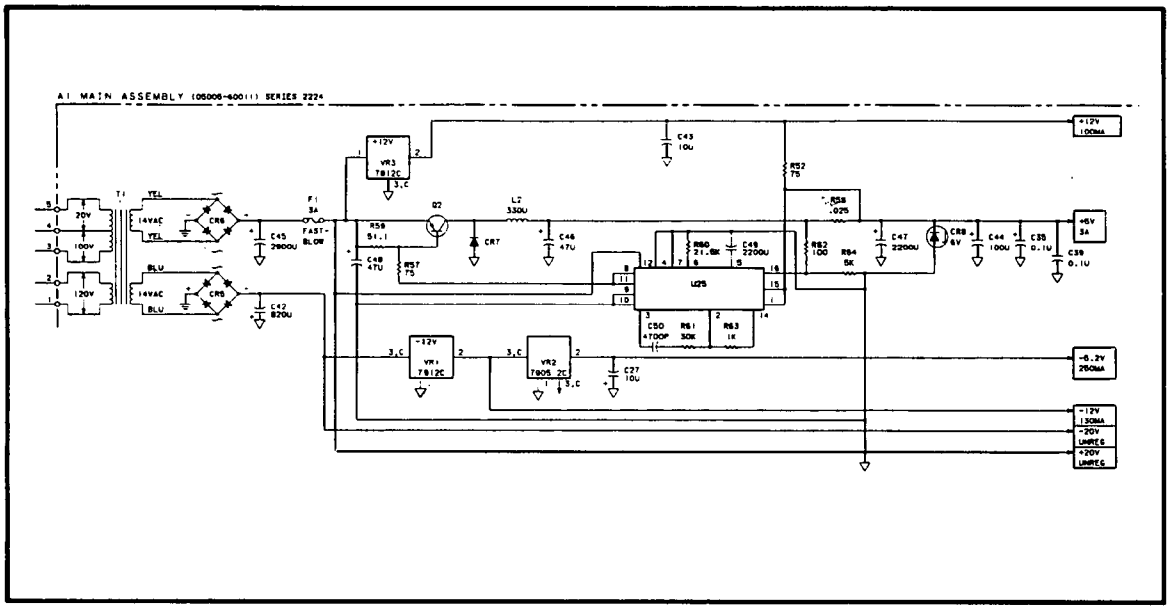
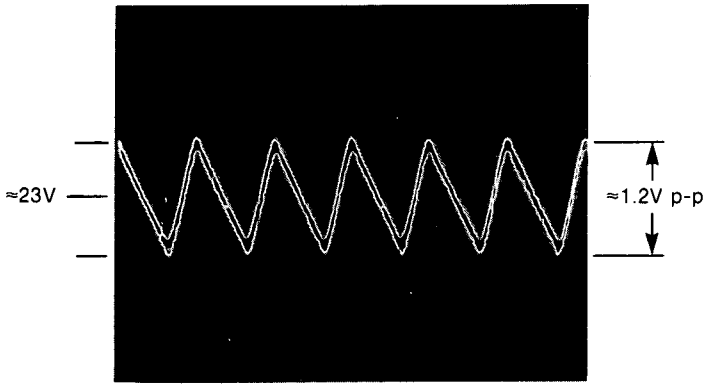
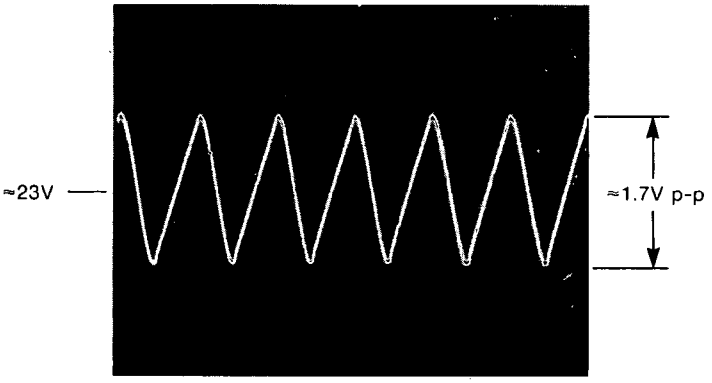


Figure 8-15. 5005B Power Supply



Volts/div. ..... .05
Time/div. ..... 5 ms
Coupling ..... AC
Probe 10:1

+20 volts unregulated for CR6 (positive output)



Volts/div. ..... .05
Time/div. ..... 5 ms
Coupling ..... AC
Probe 10:1

-20 volts unregulated for CR5 (negative output)

Figure 8-16. Power Supply Unregulated Supplies

8-287. Three of the four regulated outputs are provided by three-pin series regulators; -12V by VR1, -5.2V by VR2, and +12V by VR3. The +5 volt supply is regulated by a special switching regulator consisting of a pulse width modulation controller U25, and associated circuitry. If the input voltage to regulators is correct and any outputs are incorrect, the regulators are the probable cause (excluding the U25). If replacement of a regulator does not correct the problem, it could be caused by a shorted bypass capacitor or a bad IC. An HP 547A current tracer used in conjunction with an HP 546A logic pulser can be helpful to find the bad component.

8-288. Five Volt Supply

8-289. The five volt regulated power supply uses a switching regulator circuit. The heart of this circuit is a TL494 pulse width modulation controller (U25). The TL494 IC constantly compares the 5-volt output to its internal 5-volt reference, using the difference signal to determine the duty cycle of the switching transistor Q2. The supply is current limited to a nominal 4 amps to pin 16 of the U25, which is compared to pin 15. When the signals are equal (implying that the voltage drop across R58 and R62 are equal) the pulse circuit current-limits the output to 4 amps.

8-290. Diode CR8 is an over voltage protection diode limiting the output to 6 volts. On start-up, R52 keeps pin 1 and 15 of U25 above ground. Inductor L2 is the primary energy storage device and diode CR7 provides a current path when Q2 is shut off.

8-291. To check the operation of U25, observe the pulsed output on pin 8. It should be approximately a 10-microsecond pulse train, at a 25 kHz rate, with an amplitude of ≈20 volts p-p. Refer to the waveform in *Figure 8-17.*

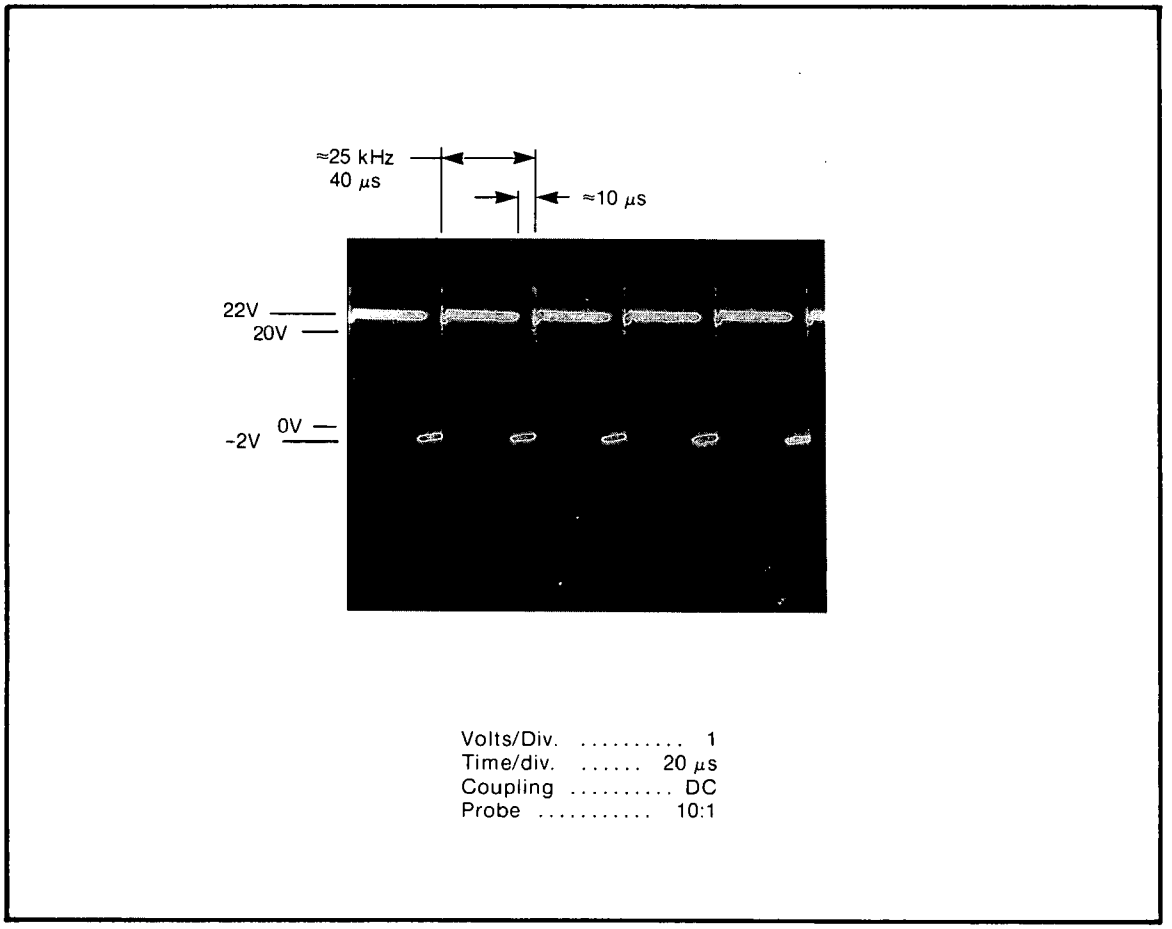


Figure 8-17. A1U25 Switching Output

8-292. KERNEL TROUBLESHOOTING

8-293. The kernel of the instrument is defined to be the power supply and the microprocessor, with its support circuitry, which comprise the minimum required logic circuitry for the 5005B's normal central processing operation.

8-294. Is the Kernel Functional?

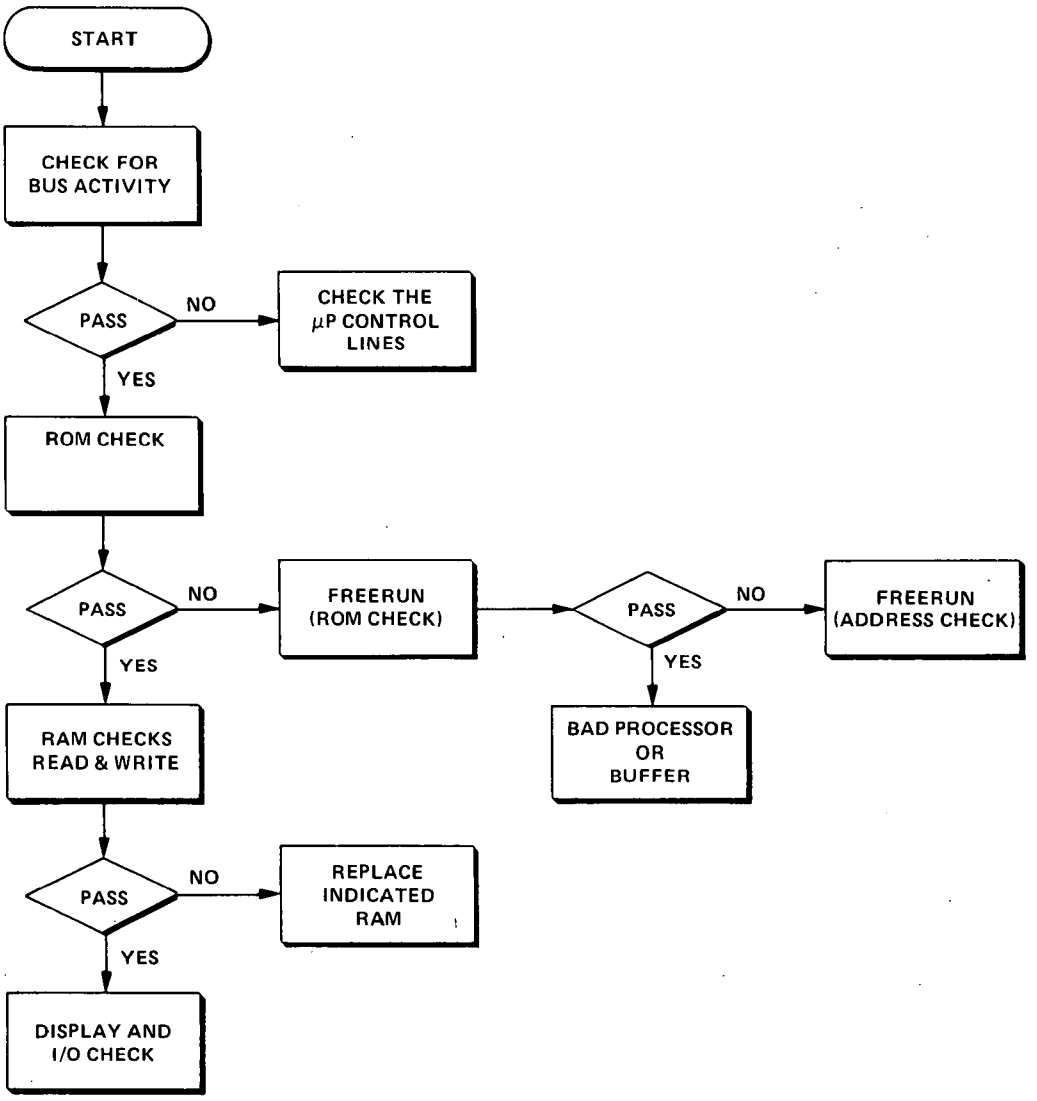
8-295. It is important to remember that all the Diagnostic routines, except Freerun (2-0), require that the kernel of the instrument be working properly. As the procedure for verification of the kernel is extensive, it is helpful to determine its status first. If the kernel can be determined to be working, the technician can proceed directly to an indicated assembly troubleshooting procedure. If, however, the initial symptoms indicate the kernel may be faulty, the technician should perform the following procedure.

8-296. Referring to the Overall Troubleshooting Flowchart, many of the initial turn-on symptoms can indicate whether the kernel is functioning or not. Error Messages, Missing Digits or Segments, or a Normal (four bars) Power-Up Self Check display are logical responses, and generally indicate the kernel is functional. For these types of symptoms the technician should bypass the Kernel troubleshooting, and proceed to an assembly procedure indicated by the flowchart. If a Blank or Hieroglyphic display appears, the operation of the kernel should be suspected. After the power supply is checked, perform the following troubleshooting tests:

TROUBLESHOOTING TEST	DIAGNOSTIC NUMBER
Bus Activity Test	—
ROM Test	0-1
RAM Read Test	0-3
RAM Write Test	0-3
Front Panel Activity Test	—
Freerun ROM Test	2-0
Freerun Address Test	2-0

Table 8-8. Kernal Troubleshooting Procedure

The following flowchart illustrates the recommended procedure for troubleshooting the kernel.



1. Perform the Bus Activity test.

   Purpose: The purpose of this test is to determine if the microprocessor has been halted by some external or internal fault condition.

   Procedure:

   a. Place a logic probe on the low order bit (AD0) of the of the microprocessor address bus (pin 12 of U16). A flashing probe indicates there is activity on the bus. If so, the bus is not halted. Proceed to step 2.

   b. A static high or low indicates that the microprocessor is being held up by some fault. Check the control lines of the microprocessor listed below, for normal activity. An explanation of the control lines is provided in paragraph 8-214.

Table 8-8. Kernal Troubleshooting Procedure (Continued)

Signal Name	Pin #	Normal Activity
1. READY	35	A non-fixed duty cycle square wave (TTL levels).
2. RST 5.5	9	Logic zero (0 volts).
3. RST 6.5	8	Logic zero (0 volts).
4. RST 7.5	7	Logic one (+5 volts).
5. RESET IN*	36	Goes LOW on power-up and then goes HIGH.
6. X1	1	5 MHz square wave.
7. X2	2	5 MHz square wave.

*Indicates a negated signal

Indications:

If the control lines all appear correct, there is a possibility that a bus buffer or other device could be holding the AD0 line. Check other Address lines/Data lines AD1 through AD15 for activity.

2. Perform the ROM test (Diag 0-1).

Purpose: The ROM test is an actual diagnostic program that verifies the microprocessor is actually receiving correct data from the ROM and that it can run a small program. This test also verifies proper operation of buffer U14.

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-1 (S1=0 S2=1).

b. Connect the test signature analyzer as follows:

Controls:

START ..... Falling edge
STOP ..... Rising edge
CLOCK ..... Rising edge

Timing Pod:

START ..... A3 TP A15
STOP ..... A3 TP A15
CLOCK ..... A3 TP $\overline{RD}$
GND ..... A3 TP GND

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

Table 8-8. Kernal Troubleshooting Procedure (Continued)

d. Verify the signatures for A3 U16, shown below.

S.A. Setup — UUT Connections

Clk: $\overline{RD}$
Start/Stop: A15
Stop Qual: A15

S.A Setup — Polarities

Clk: ⨍
Start: ⨽
Stop: ⨍

V_{CC} Signature = H559

"X" Signature = Don't Care

U16

H559	1	40	H559
0000	2	39	0000
0000	3	38	0000
0000	4	37	H559
X	5	36	H559
0000	6	35	H559
H559	7	34	4922
0000	8	33	H559
0000	9	32	X
0000	10	31	H559
H559	11	30	0000
1A6F	12	29	U525
6H9U	13	28	0000
43F6	14	27	0000
F143	15	26	0000
9P21	16	25	4303
F104	17	24	8C18
C9P7	18	23	30F6
4PA8	19	22	H3A7
0000	20	21	9FAH

Indications:

If the signatures are correct, continue with the RAM read test in step 3. If any of the signatures are incorrect, proceed to Freerun checks, beginning with step 6.

3. Perform RAM Read Test (Diag 0-3).

Purpose: The following test verifies that the RAM is capable of being written-to and read-from. If the given signatures are incorrect, perform the RAM write test to verify that a proper write is being performed on the RAM. The RAM write test should logically separate a write or control problem from a read problem.

Table 8-8. Kernal Troubleshooting Procedure (Continued)

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-3 (S1=0 S2=3).

b. Connect the test signature analyzer as follows:

Controls:

START ..... Falling edge
STOP ..... Rising edge
CLOCK ..... Rising edge

Timing Pod:

START ..... A3 TP A15
STOP ..... A3 TP A15
CLOCK ..... A3 TP $\overline{RD}$
GND ..... A3 TP GND

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

d. Verify the signatures for A3 U16 and U8, shown below.

S.A Setup — Polarities

Clk: ⨍
Start: ⨏
Stop: ⨍

S.A. Setup — UUT Connections

Clk: $\overline{RD}$
Start/Stop: A15
Stop Qual: A15

V_{CC} Signature = 1CF5

"X" Signature = Don't Care

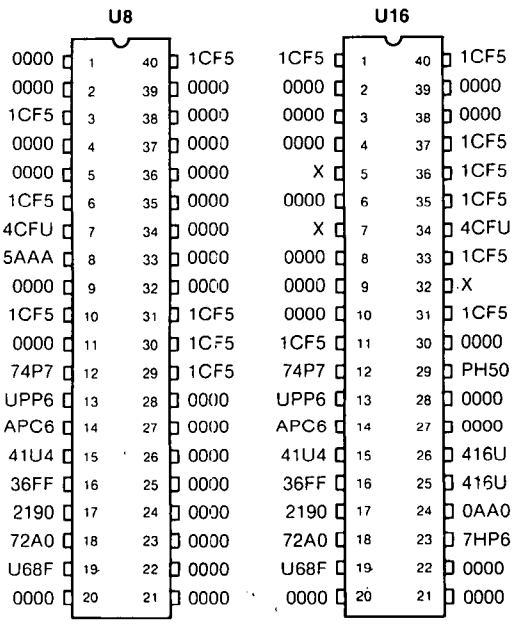


Table 8-8. Kernal Troubleshooting Procedure (Continued)

Indications:

If the given signatures are correct, the RAM is verified. Proceed to step 5. If the given signatures are incorrect, perform the RAM Write test to verify that a proper write is being performed on the RAM. The RAM Write test should logically separate a write or control problem from a read problem.

4. Perform RAM Write Test (Diag 0-3).

NOTE

This test is not necessary if the previous RAM read test performs properly.

Purpose: This test performs the same test as RAM Read but allows signatures to be taken from the Data lines when a write occurs.

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-3 (S1=0 S2=3).

b. Connect the test signature analyzer as follows:

Controls:

START ..... Falling edge
STOP ..... Rising edge
CLOCK ..... Rising edge

Timing Pod:

START ..... A3 TP A15
STOP ..... A3 TP A15
CLOCK ..... A3 TP $\overline{WR}$
GND ..... A3 TP GND

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

d. Verify the signatures for A3U16 and U8, shown below.

S.A Setup — Polarities

Clk: ⨍
Start: ⨏
Stop: ⨍

S.A. Setup — UUT Connections

Clk: $\overline{WR}$
Start/Stop: A15
Stop Qual: A15

V_{CC} Signature = 4596

"X" Signature = Don't Care

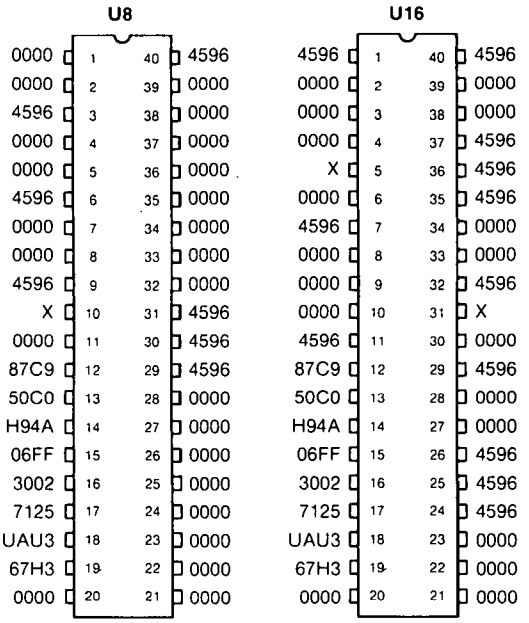


Table 8-8. Kernal Troubleshooting Procedure (Continued)

Indications:

If any of the given signatures are incorrect, suspect a bad RAM. Check for activity on the control lines; $\overline{WR}$, $\overline{CE}$, $\overline{RD}$, and IO/$\overline{M}$.

5. Check the front panel Display for activity.

   Purpose: The purpose of this test is to verify that the front panel Display is responding to the Display Decoder Driver.

   Procedure:

   a. To test for activity on the front panel display, turn the UUT to on. There should be some kind of illuminated display present. Place a logic probe on the "a through g, dp, and 1 through 8" outputs of A3U6, the Display Decoder Driver.

   b. Verify that the logic probe flashes, indicating activity, on each of the lines.

   Indications:

   If there is bus activity, and there are no segments lighted, suspect a bad ribbon cable or open/shorted V_{CC} lines on A4. No bus activity indicates A3U6 is faulty. Retrace the inputs for A3U6.

6. Perform the Freerun ROM test (Diag 2-0).

   Purpose: The purpose of the procedure is to verify the contents of all three ROMs, and data bus buffer U14.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 2-0 (S1=2 S2=0).

   b. Connect the test signature analyzer as follows:

      Controls:

      START ..... Falling edge
      STOP ..... Rising edge
      CLOCK ..... Rising edge

      Timing Pod:

      START ..... A3 TP CE1
      STOP ..... A3 TP CE3
      CLOCK ..... A3 TP $\overline{RD}$
      GND ..... A3 TP GND

   c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

   d. Verify the signatures for A3U4, shown below. If all appear correct, the contents of all the ROMs are verified. If any signatures are incorrect, first verify that the freerun pattern has been forced onto the bus by the microprocessor. Check the signatures at A3U16. If U16 signatures are correct, one of the three ROMs is bad. To determine which ROM is bad, continue this procedure.

Table 8-8. Kernal Troubleshooting Procedure (Continued)

S.A Setup — Polarities

Clk: ⨍
Start: ⨽
Stop: ⨍

S.A. Setup — UUT Connections

Clk: $\overline{\text{RD}}$
Start/Stop: CE1
Stop Qual: CE3

V_{CC} Signature = OP7C

"X" Signature = Don't Care

U4

X	1	40	0P7C
X	2	39	X
X	3	38	X
X	4	37	X
X	5	36	X
X	6	35	X
X	7	34	X
X	8	33	X
X	9	32	X
X	10	31	X
X	11	30	X
AAFP	12	29	X
5418	13	28	X
23H9	14	27	X
P30H	15	26	X
U0U3	16	25	X
HA4P	17	24	X
8H98	18	23	2338
P67C	19	22	54PF
0000	20	21	PC45

U16

0P7C	1	40	0P7C
0000	2	39	0000
0000	3	38	0000
0000	4	37	0P7C
X	5	36	0P7C
0000	6	35	0P7C
0P7C	7	34	0000
0P7C	8	33	0P7C
0000	9	32	0000
0000	10	31	0P7C
0P7C	11	30	0000
0P7C	12	29	0P7C
0P7C	13	28	X
0P7C	14	27	X
0P7C	15	26	0000
0P7C	16	25	7A70
0P7C	17	24	U81P
0P7C	18	23	2338
0000	19	22	54PF
0000	20	21	PC45

e. To verify the contents of ROM U11, connect the signature analyzer ST and SP lines to CE1 and turn the LINE switch from ON to OFF then back to ON. Verify the following signatures.

S.A Setup — Polarities

Clk: ⨍
Start: ⨽
Stop: ⨍

S.A. Setup — UUT Connections

Clk: $\overline{\text{RD}}$
Start/Stop: CE1
Stop Qual: CE1

V_{CC} Signature = 7A70

"X" Signature = Don't Care

U11

X	1	40	7A70
X	2	39	7A70
X	3	38	X
X	4	37	X
X	5	36	X
X	6	35	X
X	7	34	X
X	8	33	X
X	9	32	X
X	10	31	X
X	11	30	X
H6F0	12	29	X
6590	13	28	X
1FCC	14	27	X
1AC0	15	26	X
4HUP	16	25	X
73P3	17	24	X
H312	18	23	8P54
3F65	19	22	1734
0000	20	21	9635

Table 8-8. Kernal Troubleshooting Procedure (Continued)

f. To verify the contents of ROM U13, connect the signature analyzer ST and SP lines to CE2 and turn the LINE switch from ON to OFF then back to ON. Verify the following signatures.

S.A Setup — Polarities

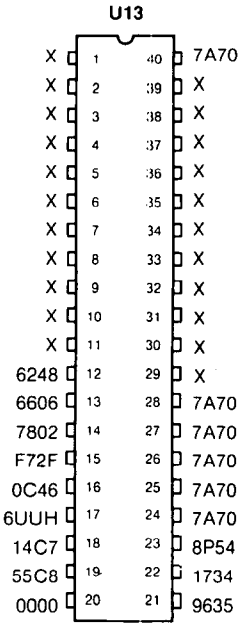
Clk: ⨍
Start: ⨾
Stop: ⨍

S.A. Setup — UUT Connections

Clk: $\overline{\text{RD}}$
Start/Stop: CE2
Stop Qual: CE2

V_{CC} Signature = 7A70

"X" Signature = Don't Care



g. To verify the contents of ROM U4, connect the signature analyzer ST and SP lines to CE3 and turn the LINE switch from ON to OFF then back to ON. Verify the following signatures.

S.A Setup — Polarities

Clk: ⨍
Start: ⨾
Stop: ⨍

S.A. Setup — UUT Connections

Clk: $\overline{\text{RD}}$
Start/Stop: CE3
Stop Qual: CE3

V_{CC} Signature = 7A70

"X" Signature = Don't Care

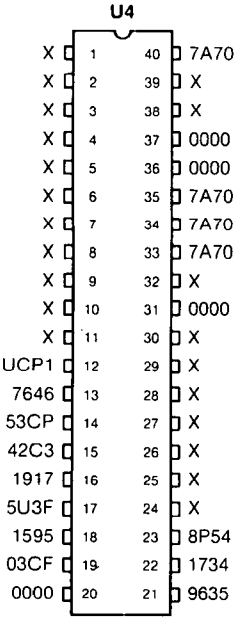


Table 8-8. Kernal Troubleshooting Procedure (Continued)

7. Perform the Freerun Address Check (Diag 2-0).

   Purpose: The purpose of this test is to verify the address selection and decoding lines from the kernel. It places the microprocessor in a freerun address loop, allowing stable signatures on the kernel outputs.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 2-0 (S1=2 S2=0).

   b. Connect the test signature analyzer as follows:

      Controls:

      START ..... Rising edge
      STOP ..... Rising edge
      CLOCK ..... Falling edge

      Timing Pod:

      START ..... A3 TP A15
      STOP ..... A3 TP A15
      CLOCK ..... A3 TP ALE
      GND ..... A3 TP GND

   c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

   d. Verify the signatures for A3U4, shown below.

S.A Setup — Polarities

Clk: ↓
Start: ↓
Stop: ↓

S.A. Setup — UUT Connections

Clk: ALE
Start/Stop: A15
Stop Qual: A15

V_{CC} Signature = 0001

"X" Signature = Don't Care

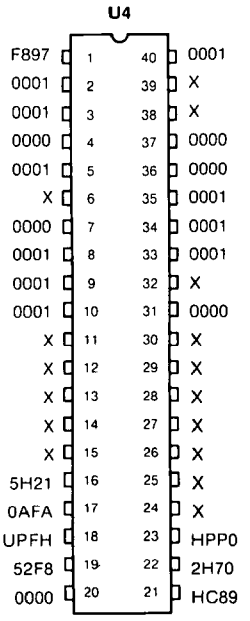


Table 8-8. Kernal Troubleshooting Procedure (Continued)

Indications:

If any of the signatures are incorrect, try to backtrace the faults by taking previous path signatures. A majority of the A3 IC signatures for this diagnostic mode are given below.

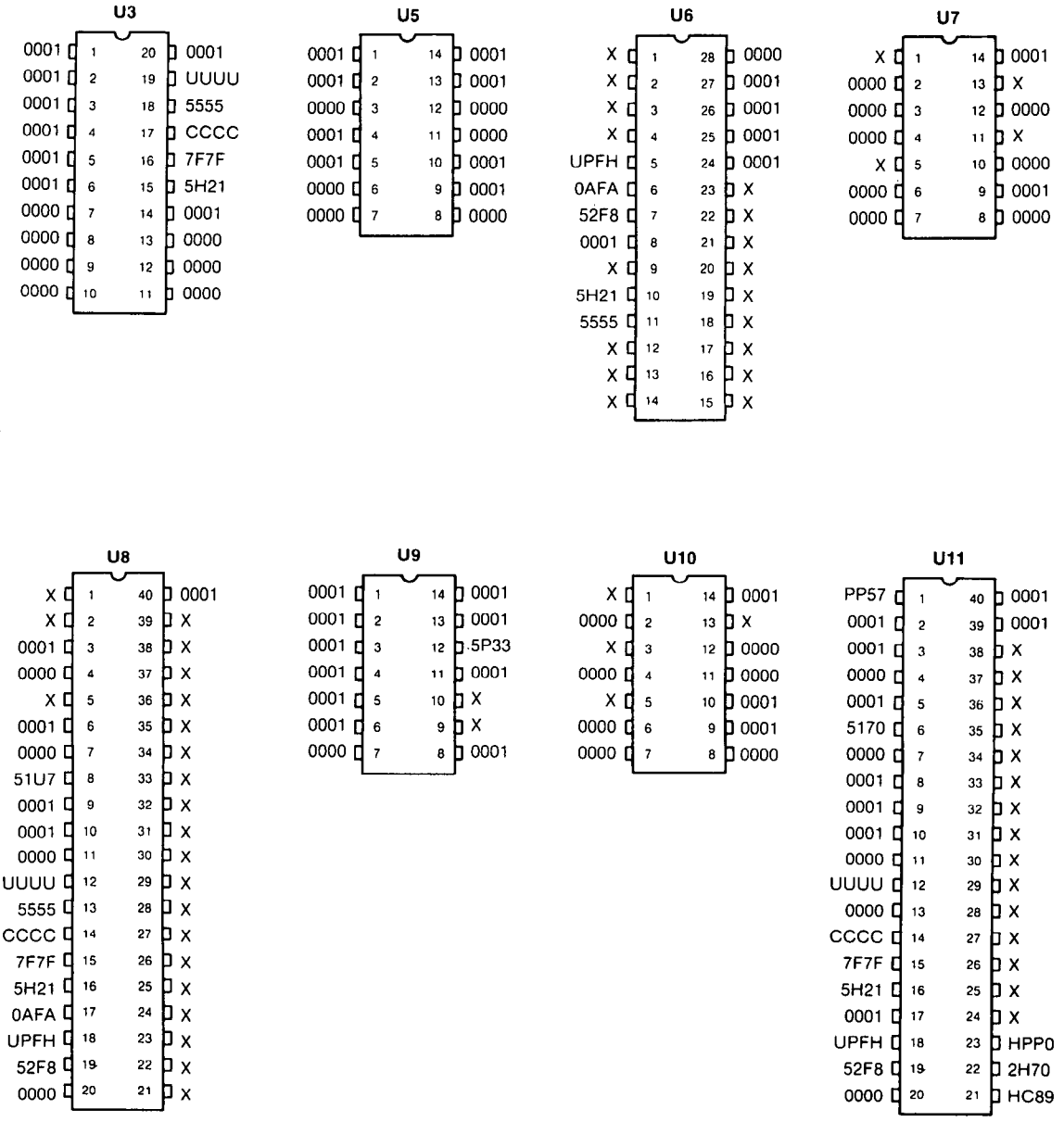
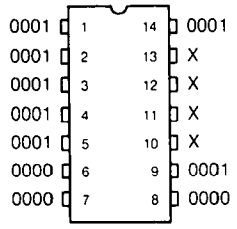
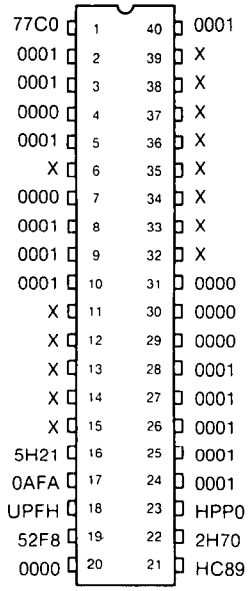


Table 8-8. Kernal Troubleshooting Procedure (Continued)

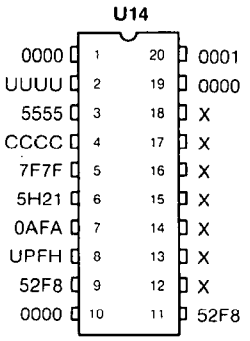
U12



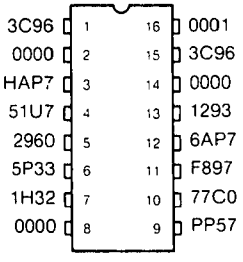
U13



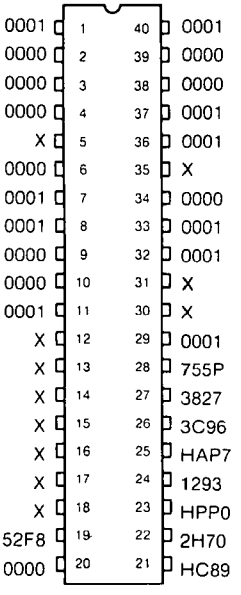
U14



U15



U16



8-297. A1 TROUBLESHOOTING

8-298. The A1 Main Assembly contains the Signature Analyzer circuitry, the Frequency and Time Interval Counter, the Digital to Analog Converters, and the Logic selector circuits.

8-299. The following tests verify specific circuits within the A1 assembly. As each test is performed, the operative status of the indicated circuits is determined. Perform the tests in the order given. The A1 troubleshooting tests are:

TROUBLESHOOTING TEST	DIANOSTIC NUMBER
Input Voltage Comparators	—
Signature Analyzer Diag NORM	0-6
Signature Analyzer Diag TEST	0-6
Counter Diag	0-7
Time Interval Diag	0-8
DAC Static Output Diags	0-9, 0-A, 0-B, 0-C
DAC Dynamic Ramp Diag	0-D
V_P+ Zero Offset Diag	0-E
V_P– Zero Offset Diag	0-F

Table 8-9. A1 Troubleshooting Procedure

1. Perform the Input Voltage Comparator Test.

   Purpose: The Input Voltage Comparator Test provides a method of verifying the operation of the Data Probe, Timing Pod, Input Compensation circuitry and Input Voltage Comparators. These front end circuits are analog configurations, which are beyond the capabilities of the self diagnostic test routines built into the 5005B.

   Procedure:

   a. Set the 5005B to the kΩ mode. With the 5005B Data Probe, measure the resistance between ground and each Timing Pod input. The GND input should read 0.000; the START/ST-SP, STOP/QUAL, and CLOCK inputs should each read approximately 98 KΩ.

   b. Set up a pulse generator for a 10 kHz TTL square wave. Connect the output to the Data Probe tip. Remember to connect the probe ground lead. Using an oscilloscope, trace the signal from the Data Probe tip, through A1U6(A and B), to the ECL to TTL translators. The signal should be easily traceable, in any function mode, with a reasonable TTL square wave out of the translator.

   c. Repeat for START/ST/SP, STOP/QUAL, and CLOCK inputs of the Timing Pod.

   Indications:

   A test signal should be traceable from any of the instrument inputs through its respective level translator. The signal level changes from TTL to ECL (out of the Input Voltage Comparator), and back to TTL (out of the translator). If the shape of the square wave appears suspiciously rounded or mishapen, refer to paragraph 5-13, Input Compensation Adjustments. If the signal does not appear out of the translator, check the ECL output of the Voltage Comparator.

2. Perform the Signature Analyzer NORM Diagnostic (Diag 0-6).

   Purpose: The Signature Analyzer NORM Diagnostic provides the user with "key signatures", which help quickly verify the signature analyzer circuits. Checking these key signatures first will insure functionality of the signature analyzer circuitry. If the following signatures are correct, the signature analyzer portion of the circuitry can be assumed to be properly functioning. If any of the key signatures are incorrect, backtrace through the A1 assembly.

Table 8-9. A1 Troubleshooting Procedure (Continued)

Procedure:

a. Set the diagnostic rotary switches on A3 to 0-6 (S1=0 S2=6).

b. Connect the test signature analyzer as follows:

Controls:

START ..... Falling edge
STOP ..... Rising edge
CLOCK ..... Rising edge

Timing Pod:

START ..... A3 TP A15
STOP ..... A3 TP A15
CLOCK ..... A3 TP $\overline{RD}$
GND ..... A3 TP GND

c. Connect the 5005B (UUT) as follows:

Timing Pod:

START/ST/SP ..... A3 TP ST
STOP/QUAL ..... A3 TP SP
CLOCK ..... A3 TP CLK
(GND) ..... A3 TP GND
Data Probe ..... A3 TP DATA

d. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

CAUTION

This test rapidly opens and closes relays on the A1 Main Assembly. Extended running of this test could cause the relays to fail. Run the test only while necessary.

e. Verify that the light within the UUT Data Probe turns off when the probe tip is grounded, and lights brightly when the probe tip is connected to +5 volts. The test signature analyzer should display the signature "HH03" for +5 volts.

f. With the data probe from the test signature analyzer, verify the following Key Signatures:

Assembly	Component	Pin #	Signature
A3 Microprocessor	U4	34	C0H4
A3 Microprocessor	U10	5	APPP
A3 Microprocessor	U4	37	2U48
A3 Microprocessor	U4	35	60AH
A3 Microprocessor	U4	36	85C2
A3 Microprocessor	J1	$\overline{16}$	HH03 (10 MHz)

Indications:

If one or more of the key signatures are incorrect, use a half-splitting or back-tracing technique to locate the bad node in the circuit. The A1 assembly signatures for this diagnostic mode are listed on the following pages.

NOTE

A1U6 is an ECL type device. Signatures taken on A1U6 must be done with a test signature analyzer with ECL data threshold capability.

Table 8-9. A1 Troubleshooting Procedure (Continued)

S.A. Setup — Polarities

Clk: ⨍
Start: ⨍
Stop: ⨍

S.A. Setup — UUT Connections

Clk: RD*
Start/Stop: A15
Stop Qual: A15

V_{CC} Signature = HH03

"X" Signature = Don't Care

U2

7C10	1	16	HH03
CC32	2	15	0000
6H83	3	14	0000
CFF9	4	13	F526
820C	5	12	F526
HC1F	6	11	HH03
43FH	7	10	1825
0000	8	9	HH03

U3

0000	1	16	HH03
U288	2	15	0000
HH03	3	14	0716
8376	4	13	CHC8
✓60AH	5	12	CHC8
0000	6	11	5PFU ✓
✓9225	7	10	H8U0
0000	8	9	3P4H ✓

U5

0000	1	16	HH03
2F96	2	15	9225
2F96	3	14	5A70
0000	4	13	7P88
HH03	5	12	C6HH
3CFH	6	11	5U2C
P6FP	7	10	8786
0000	8	9	6P70

U6

X	1	24	1595
X	2	23	1595
X	3	22	X
X	4	21	X
X	5	20	X
X	6	19	X
X	7	18	X
X	8	17	FU6F
X	9	16	X
9604	10	15	X
4115	11	14	X
X	12	13	X

U8

1825	1	16	HH03
3P4H	2	15	0000
7P88	3	14	136P
136P	4	13	A0H8
A0H8	5	12	HC94
HC94	6	11	5U2C
HH03	7	10	U288
0000	8	9	X

U9

1825	1	16	HH03
3P4H	2	15	CH8F
6P70	3	14	P7PP
P7PP	4	13	63U7
63U7	5	12	5A70
5A70	6	11	C214
0000	7	10	HH03
0000	8	9	X

U10

1PC8	1	14	HH03
1825	2	13	8CUP
3CCC	3	12	PH06
U24C	4	11	3CCC
2U48	5	10	F526
U24C	6	9	1825
0000	7	8	F526

U11

0000	1	16	0000
0000	2	15	0000
0000	3	14	0000
1595	4	13	4115
126U	5	12	9604
0000	6	11	0000
0000	7	10	0000
0000	8	9	HH03

U12

0000	1	16	0000
0000	2	15	0000
0000	3	14	0000
126U	4	13	FU6F
F896	5	12	1595
0000	6	11	0000
0000	7	10	0000
0000	8	9	HH03

*Set data thresholds on test equipment to ECL logic levels.

Table 8-9. A1 Troubleshooting Procedure (Continued)

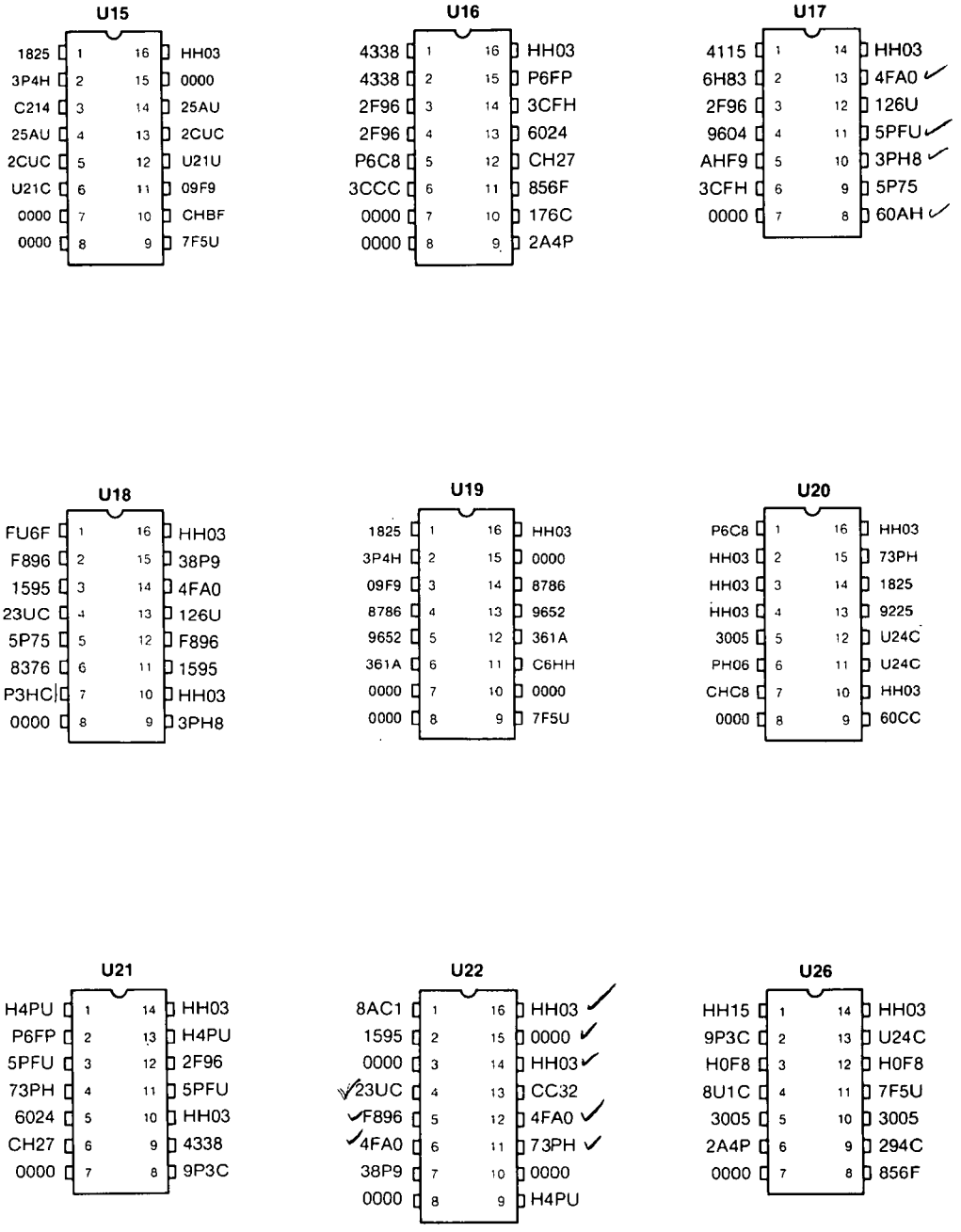


Table 8-9. A1 Troubleshooting Procedure (Continued)

3. Perform the Signature Analyzer Test Diagnostic (Diag 0-6).

   Purpose: The Signature Analyzer Test Diagnostic uses the S.A. Test switches on the A3 assembly to tie selected data lines either high (to +5 volts) or low (to ground). These conditions, along with the diagnostic mode, force the FSR into a closed loop which generates stable signatures.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 0-6 (S1=0 S2=6).

   b. Connect the test signature analyzer as follows:

      Controls:

      START ..... Falling edge
      STOP ..... Rising edge
      CLOCK ..... Rising edge

      Timing Pod:

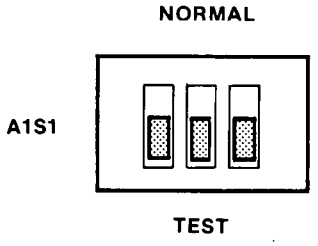
      START ..... A3 TP A15
      STOP ..... A3 TP A15
      CLOCK ..... A3 TP $\overline{RD}$
      GND ..... A3 TP GND

   c. Connect the 5005B (UUT) as follows:

      Timing Pod:

      START/ST/SP ..... A3 TP ST
      STOP/QUAL ..... A3 TP SP
      CLOCK ..... A3 TP CLK
      (GND) ..... A3 TP GND
      Data Probe ..... A3 TP DATA

   d. Set all three sections of S.A. Test switch A1S1 to the Test position.



   e. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

CAUTION

This test rapidly opens and closes relays on the A1 Main Assembly. Extended running of this test could cause the relays to fail. Run the test only while necessary.

Table 8-9. A1 Troubleshooting Procedure (Continued)

f. Verify the signatures on the individual inputs and outputs of the Feedback Shift Register, as shown below:

S.A Setup — Polarities

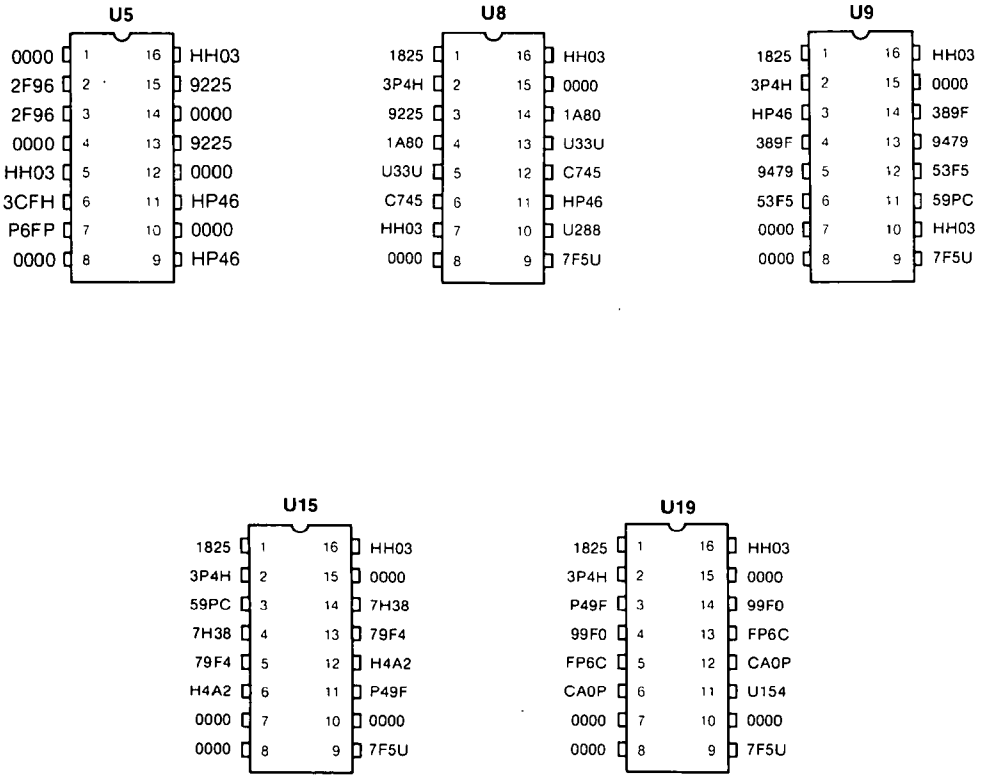
Clk: ⨍
Start: ⨽
Stop: ⨍

S.A. Setup — UUT Connections

Clk: $\overline{RD}$
Start/Stop: A15
Stop Qual: A15

V_{CC} Signature = HH03

"X" Signature = Don't Care



Indications:

This closed loop allows the verification of each input and output of the four registers which comprise the Feedback Shift Register. An incorrect signature indicates a faulty device or problem with the printed circuit trace.

NOTE

Be sure to return the Test Switches (A1S1) to their NORMAL positions after testing.

Table 8-9. A1 Troubleshooting Procedure (Continued)

4. Perform the Counter Diagnostic (Diag 0-7).

   Purpose: The counter diagnostic exercises nodes on U5, U8, U9, U15, and U19 on the A1 Mainboard, which are not exercised by the signature analyzer diagnostic. The test is initiated as follows:

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 0-7 (S1=0 S2=7).

   b. Connect the test signature analyzer as follows:

      Controls:

      START ..... Falling edge
      STOP ..... Rising edge
      CLOCK ..... Rising edge

      Timing Pod:

      START ..... A3 TP A15
      STOP ..... A3 TP A15
      CLOCK ..... A3 TP $\overline{RD}$
      GND ..... A3 TP GND

   c. Connect the 5005B (UUT) as follows:

      Timing Pod:

      START/ST/SP ..... A3 TP ST
      STOP/QUAL ..... A3 TP SP
      CLOCK ..... A3 TP RD CLK
      GND ..... A3 TP GND
      Data Probe ..... A3 TP DATA

   d. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

      CAUTION

      This test rapidly opens and closes relays on the A1 Main Assembly. Extended running of this test could cause the relays to fail. Run the test only while necessary.

   e. Place the test signature analyzer data probe on a +5 volt TP within the UUT and verify:

      +5 volts 1299

   f. The key signature for this diagnostic is on U19 pin 11 (on the A1 Mainboard). This signature should be "911P".

      NOTE

      This test takes several seconds for each pass.

Table 8-9. A1 Troubleshooting Procedure (Continued)

Indications:

If the key signature is incorrect, use the schematic diagram and the following signatures to determine which of the counter integrated circuits is faulty.

S.A Setup — Polarities

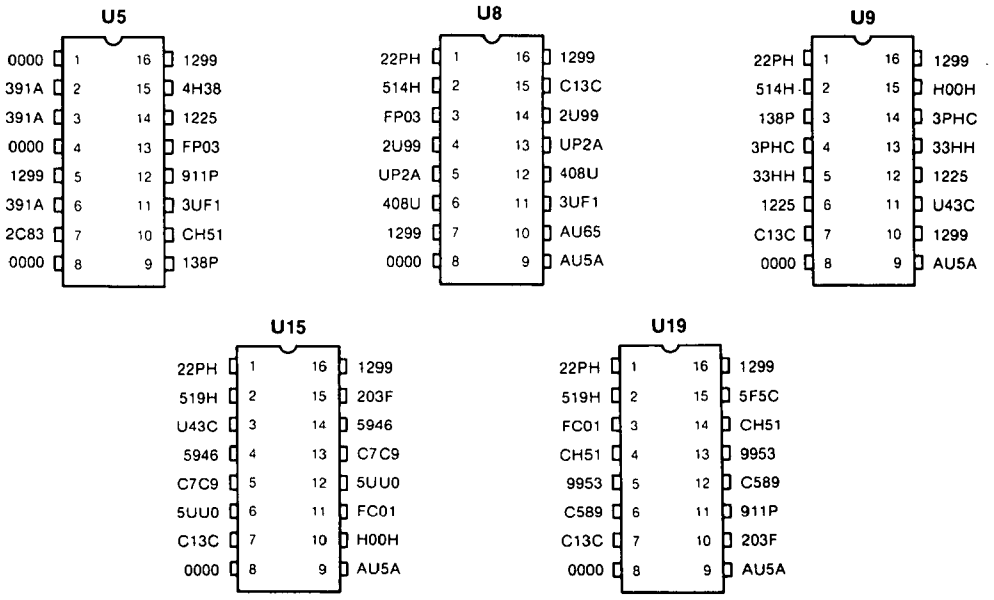
Clk: ↓
Start: ↑
Stop: ↓

S.A. Setup — UUT Connections

Clk: $\overline{RD}$
Start/Stop: A15
Stop Qual: A15

V_{CC} Signature = 1299

"X" Signature = Don't Care



5. Perform the Time Interval Diagnostic (Diag 0-8).

   Purpose: The Time Interval Diagnostic is similar to the Counter test, in that it places the four FSR counter ICs in a closed loop for testing. In this mode, however, data selector A1U3 is configured to direct the 10 MHz internal clock into the counter chain, while supplying an arbitrary gate. This test verifies the counter ICs and A1U3 in the T.I. mode of operation.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 0-8 (S1=0 S2=8).

   b. Connect the test signature analyzer as follows:

      Controls:

      START ..... Falling edge
      STOP ..... Rising edge
      CLOCK ..... Rising edge

      Timing Pod:

      START ..... A3 TP A15
      STOP ..... A3 TP A15
      CLOCK ..... A3 TP $\overline{RD}$
      GND ..... A3 TP GND

Table 8-9. A1 Troubleshooting Procedure (Continued)

c. Connect the 5005B (UUT) as follows:

Timing Pod:

START/ST/SP ..... A3 TP ST
STOP/QUAL ..... A3 TP SP
CLOCK ..... A3 TP CLK
(GND) ..... A3 TP GND
Data Probe ..... A3 TP DATA

d. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

e. Observe the display of the UUT. It should show a display of "1.854X", flashing at a rapid rate.

Indications:

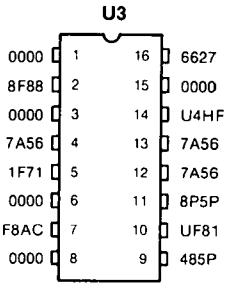
If the display appears as described above, the test is passed. Proceed to the next diagnostic. If not, check A1U3 (pin 3) for a 10 MHz TTL square wave. If the square wave is present, check A1U3 for the following signatures:

S.A Setup — Polarities
Clk: ⨍
Start: ⨽
Stop: ⨍

S.A. Setup — UUT Connections
Clk: RD
Start/Stop: A15
Stop Qual: A15

V_{CC} Signature = 6627

"X" Signature = Don't Care



6. Perform the DAC Static Output Diagnostics (Diags 0-9 through 0-C).

Purpose: The four diagnostics, which make up the DAC static output test, instruct the microprocessor to program preselected dc voltages into all four DACs U1, U4, U7, and U13 (on the A1 assembly). The voltages can be measured on TP's 1, 2, 3, and 4 on A1, and should be within ±1% of the programmed value. The four diagnostics shift the programmed voltages to each of the four DACs, as indicated in the table below.

Procedure:

a. Sequentially set the diagnostic rotary switches on A3 to each of the four positions listed below. For each position, measure the dc voltage at TP's 1, 2, 3, and 4. Remember to turn the UUT LINE switch from ON to OFF then back to ON again, each time a new diagnostic is selected.

A3S1	A3S2	A1U1 (A1TP1)	A1U4 (A1TP2)	A1U7 (A1TP3)	A1U13 (A1TP4)
0	9	0.0V	+7.65V	0.45V	-7.65V
0	A	-7.65V	0.0V	+7.65V	0.45V
0	B	0.45V	-7.65V	0.0V	+7.65V
0	C	+7.65V	0.45V	-7.65V	0.0V

Table 8-9. A1 Troubleshooting Procedure (Continued)

Indications:

This test gives a static indication of the programmability and accuracy of each of the four DACs. The inputs of all four DACs are configured in parallel. Address decoder U2A enables each DAC. If any of the DAC voltages are incorrect, check the Current-to-Voltage translators U14, A-D, and the indicated DAC output.

7. Perform the DAC Dynamic Ramp Diagnostic (Diag 0-D).

Purpose: The DAC Dynamic Ramp diagnostic instructs the microprocessor to program all four DACs to output a ramp waveform. The ramp cycles from +7.65 volts to -7.65 volts. By observing the output of each DAC, the accuracy and linearity can be monitored.

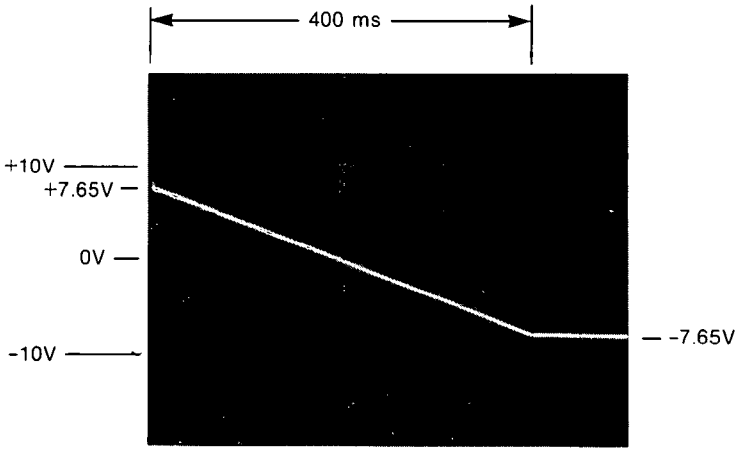
Procedure:

a. Set the diagnostic rotary switches on A3 to 0-D (S1=0 S2=D).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

c. Connect an oscilloscope to each of the four DAC test points in turn, and observe the ramp outputs. The outputs from the DACs can be obtained as a voltage waveform at the following test points:

A1U1 = TP1 A1U4 = TP2 A1U7 = TP3 A1U13 = TP4



Scope:

Volts/div	0.5V (10:1)
Time/div	50 ms
Coupling	DC
Auto/Norm	(NORM)
Trigger	+ Slope

Indications:

By setting the voltage sensitivity, vertical position, and horizontal position controls, the different areas of the waveform can be viewed. This allows checks for missing levels and nonlinearities.

Note that the smallest increment on the stairstep waveform should be 30 mV in height. The 0-volt level is displayed twice i.e., lasts twice as long as the other levels.

Table 8-9. A1 Troubleshooting Procedure (Continued)

8. Perform the V_P+ Zero Offset Value Diagnostic (Diag 0-E).

   Purpose: The V_P+ Test finds the offset value necessary to zero the V_P+ circuits. The microprocessor first programs A1K2 Data Switch Relay to the calibration position. The microprocessor programs DAC A1U1 to a starting voltage level and checks the DATA (PROBE) line from the Mainboard to establish if a transition on the input comparators has occurred. If not, the microprocessor increments the program value to the DAC, until a transition occurs. This value is established to be the zero offset value for the comparators and DACs. This value is sent to the display.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 0-E (S1=0 S2=E).

   b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

   CAUTION

   This test rapidly opens and closes relays on the A1 Main Assembly. Extended running of this test could cause the relays to fail. Run the test only while necessary.

   c. The display should contain a reading between -0.10 and 0.10.

   Indications:

   If a zero offset between -0.10 and +0.10 volts is not obtained, the display will usually contain a +12.50 or -12.50 result. This indicates that the diagnostic program did not recognize a transition, and continued stepping to its programmable limits. If this happens, try the procedure again. If it is still bad, monitor the output of A1U12 for a transition while repeating the diagnostic. Follow the transition through the A1 circuitry to DATA (PROBE) J1 pin $\overline{28}$.

9. Perform the V_P- Zero Offset Value Diagnostic (Diag 0-F).

   Purpose: The V_P- Test finds the offset value necessary to zero the V_P- circuits. The microprocessor first programs A1K2 Data Switch Relay to the calibration position. The microprocessor programs DAC U1 to a starting voltage level and checks the DATA (PROBE) line from the Mainboard to establish if a transition on the input comparators has occurred. If not the microprocessor increments the program value to the DAC, until a transition occurs. This value is established to be the zero offset value for the comparators and DACs. This value is sent to the display.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 0-F (S1=0 S2=F).

   b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

   CAUTION

   This test rapidly opens and closes relays on the A1 Main assembly. Extended running of this test could cause the relays to fail. Run the test only while necessary.

   c. The display should contain a reading between -0.10 and 0.10.

   Indications:

   If a zero offset between -0.10 and +0.10 volts is not obtained, the display will usually contain a +12.50 or -12.50 result. This indicates that the diagnostic program did not recognize a transition, and continued stepping to its programmable limits. If this happens, try the procedure again. If it is still bad, monitor the output of A1U12 for a transition while repeating the diagnostic. Follow the transition through the A1 circuitry to DATA (PROBE) J1 pin $\overline{28}$.

8-300. A2 DVM TROUBLESHOOTING

CAUTION

The DVM board is sensitive to fingerprints and other contamination. Do not handle board with bare fingers except at the edges. Contamination can cause malfunctions in the DVM circuitry.

8-301. The following tests verify specific circuits within the A2 assembly. As each test is performed, the operative status of the indicated circuits is determined. Perform the tests in the order given. Read the complete test description before initiating any DVM diagnostics. The A2 troubleshooting tests are:

TROUBLESHOOTING TEST	DIAGNOSTIC NUMBER
Test Point Measurements	—
Zero Offset Value/25V range	1-0
Zero Offset Value/250V range	1-3
Auto-Calibration/25V range	1-1
Auto-Calibration/250V range	1-4
Uncorrected Reading/25V range	1-2
Uncorrected Reading/250V range	1-5
Zero Offset Value/Ohms Mode	1-6
Reference Voltage/Ohms Mode	1-7
Measured Voltage/Ohms Mode	1-8
Overvoltage Detector Test	—

8-302. Prior to troubleshooting the A2 DVM assembly, it is recommended that the technician read and understand the DVM theory of operation given in this section.

Table 8-10. A2 Troubleshooting Procedures

1. Perform the Test Point Measurements.

   Purpose: The following two tests provide preliminary verification that the DVM reference voltage (+10.00V) and the assembly subclock signals are present.

   Procedure:

   a. Connect a dc voltmeter to the A2 assembly as follows: positive (red) lead to TP1, and negative (black) to TP2. The dc voltage should be 10.000 volts, ±1 mV. If the voltage is only slightly off, attempt to adjust using A2R2.

   b. With a frequency counter, measure the frequency of the TTL subclock signal at A2U7 pin 8. This is the 10 MHz main clock, divided by a factor of "61". The output frequency should be ≈163.93 kHz. If the frequency is incorrect, check the 10 MHz main clock input at U8 pin 2. The output of U8 pin 15 should be 655.73 kHz.

   Indications:

   If a fault is located at these areas, use the schematic to locate the problem and correct before checking for further faults.

Table 8-10. A2 Troubleshooting Procedures (Continued)

2. Zero Offset Value for 25 Volt Range (Diag 1-0).

   Purpose: The purpose of the Zero Offset Value diagnostic is to instruct the microprocessor to force the DVM assembly into the 25V range, and ground the input. The resultant voltage measurement represents the offset voltage at zero volts for the 25V range. The diagnostic activates the range and grounds the input through the Analog Crosspoint Switch. The measured offset is displayed during the test.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 1-0 (S1=1 S2=0).

   b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

   c. Verify that the 5005B displays a zero offset value between -0020. and +0020.

   Indications:

   If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be ground). Check the status of Q3 and Q4 (Q4 should be on, Q3 should be off). Check the Data/Cal relay (it should be in the CAL position).

3. Zero Offset Value for 250 Volt Range (Diag 1-3).

   Purpose: The purpose of the Zero Offset Value diagnostic is to instruct the microprocessor to force the DVM assembly into the 250V range, and ground the input. The resultant voltage measurement represents the offset voltage at zero volts for the 250V range. The diagnostic activates the range and grounds the input through the Analog Crosspoint Switch. The measured offset is displayed during the test.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 1-3 (S1=1 S2=3).

   b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

   c. Verify that the 5005B displays a zero offset value between -0020. and +0020.

   Indications:

   If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be ground). Check the status of Q3 and Q4 (Q3 should be on, Q4 should be off). Check the Data/Cal relay (it should be in the CAL position).

4. AUTO-CAL for 25 Volt Range (Diag 1-1).

   Purpose: The purpose of the Auto-Cal diagnostic is to instruct the microprocessor to force the DVM assembly into the 25V range, and connect the input to the 10.00-volt precision reference. The resultant voltage measurement represents the DVM voltage value with a known input voltage (+10.00). The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 1-1 (S1=1 S2=1).

   b. Turn the UUT LINE switch from ON to OFF then back back to ON. This initiates the diagnostic.

   c. Verify that the 5005B displays an Auto-Cal value between 09500. and 10100.

   Indications:

   If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be +10.00V). Check the status of Q3 and Q4 (Q3 should be on, Q4 should be off). Check the Data/Cal relay (it should be in the CAL position).

5. AUTO-CAL For 250 Volt Range (Diag 1-4).

   Purpose: The purpose of the Auto-Cal diagnostic is to instruct the microprocessor to force the DVM assembly into the 250V range, and connect the input to the +10.00 volt precision reference. The resultant voltage measurement represents the DVM voltage value with a known input voltage (+10.00). The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

Table 8-10. A2 Troubleshooting Procedures (Continued)

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-4 (S1=1 S2=4).

b. Turn the UUT LINE switch from ON to OFF then back back to ON. This initiates the diagnostic.

c. Verify that the 5005B displays an Auto-Cal value between 00940. and 01020.

Indications:

If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be +10.00V). Check the status of Q3 and Q4 (Q3 should be on, Q4 should be off). Check the Data/Cal relay (it should be in the CAL position).

6. Uncorrected Reading For The 25 Volt Range (Diag 1-2).

Purpose: The purpose of the uncorrected reading diagnostic is to instruct the microprocessor to force the DVM assembly into the 25V range, and connect the input to the Data Probe path. The resultant voltage measurement represents the DVM voltage value through the Data Probe path. The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

The microprocessor enables the voltage probe path and continuously measures the probe tip voltage. This raw voltage measurement is sent to the microprocessor. No arithmetic is performed. The raw measurement value is sent to the display. This is a test of the probe capability to measure a raw voltage properly. Note that the displayed voltage will not be the actual voltage present at the tip due to offsets and scaling. The formula for computing the actual voltage at the probe tip is:

$$\text{Voltage at Tip} = \frac{\text{Uncorrected reading - Zero offset}}{\text{10.00 volt ref reading - Zero offset}} \text{ X10V}$$

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-2 (S1=1 S2=2).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

c. Verify that the 5005B displays an uncorrected DVM value within the allowable tolerance, as defined above.

Indications:

If the display contains an incorrect result, check the status of A2K2 (it should be in the DATA position). Check the status of Q3 and Q4 (Q3 should be on, Q4 should be off).

7. Uncorrected Reading For The 250 Volt Range (Diag 1-5).

Purpose: The purpose of the uncorrected reading diagnostic is to instruct the microprocessor to force the DVM assembly into the 250V range, and connect the input to the Data Probe path. The resultant voltage measurement represents the DVM voltage value through the Data Probe path. The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

The microprocessor enables the voltage probe path and continuously measures the probe tip voltage. This raw voltage measurement is sent to the microprocessor. No arithmetic is performed. The raw measurement value is sent to the display. This is a test of the probe capability to measure a raw voltage properly. Note that the displayed voltage will not be the actual voltage present at the tip due to offsets and scaling. The formula for computing the actual voltage at the probe tip is:

$$\text{Voltage at Tip} = \frac{\text{Uncorrected reading - Zero offset}}{\text{10.00 volt ref reading - Zero offset}} \text{ X10V}$$

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-5 (S1=1 S2=5).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

c. Verify that the 5005B displays an uncorrected DVM value within the allowable tolerance, as defined above.

Indications:

If the display contains an incorrect result, check the status of A2K2 (it should be in the DATA position). Check the status of Q3 and Q4 (Q3 should be on, Q4 should be off).

Table 8-10. A2 Troubleshooting Procedures (Continued)

8. Zero Offset Value For Ohms (Diag 1-6).

   Purpose: The purpose of the Zero Offset Value diagnostic is to instruct the microprocessor to force the DVM assembly into the 2.5V range (Ohms only), and ground the input. The resultant voltage measurement represents the offset voltage at zero volts for the Ohms mode. The diagnostic activates the range and grounds the input through the Analog Crosspoint Switch. The measured offset is displayed during the test.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 1-6 (S1=1 S2=6).

   b. Turn the UUT LINE switch from ON to OFF then back back to ON. This initiates the diagnostic.

   c. Verify that the 5005B displays a zero offset value between -0020. and +0020.

   Indications:

   If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be ground). Check the status of Q3 and Q4 (Q4 and Q3 should both be off). Check the Data/Cal relay (it should be in the CAL position).

9. Reference Voltage For Ohms (Diag 1-7).

   Purpose: The purpose of the reference voltage diagnostic is to instruct the microprocessor to force the DVM assembly into the 2.5V range (Ohms only), and connect the input to the +2.0 volt Reference. The resultant voltage measurement represents the DVM -2.0 volt reference value for the Ohms mode. The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 1-7 (S1=1 S2=7).

   b. Turn the UUT LINE switch from ON to OFF then back back to ON. This initiates the diagnostic.

   c. Verify that the 5005B displays an Ohms reference value between 19500 and 20500.

   If the display contains an incorrect result, check the status of A2U2 pin 9 (it should be +2.00 volts). Check the status of Q3 and Q4 (Q4 and Q3 should both be off). Check the status of A2K2 (it should be in the CAL position).

10. Measure Voltage for Ohms (Diag 1-8).

    Purpose: The purpose of the measure voltage diagnostic is to instruct the microprocessor to force the DVM assembly into the 2.5V range (Ohms mode), connect the DVM input to the Data Probe path, and connect the +2.0 volt current source, through K1, to the Data Probe reference resistor. The resultant voltage measurement represents the DVM reference voltage value through the Data Probe path. The diagnostic activates the range and connects the input through the Analog Crosspoint Switch. The measured value is displayed during the test.

    The microprocessor enables the voltage probe path and continuously measures the voltage through the probe reference resistance. This raw voltage measurement is sent to the microprocessor. No arithmetic is performed. The raw measurement value is sent to the display. This is a test of the probe capability to measure a raw voltage properly. Note that the displayed voltage will not be the actual voltage present at the tip due to offsets and scaling.

    Procedure:

    a. Set the diagnostic rotary switches on A3 to 1-8 (S1=1 S2=8).

    b. Turn the UUT LINE switch from ON to OFF then back back to ON. This initiates the diagnostic.

    c. Verify that the 5005B displays an Ohms reference value between -0020. and +0020.

    Indications:

    If the display contains an incorrect result, check the status of A2K2 and K1 (K2 in CAL, K1 closed). Check the status of Q3 and Q4 (Q4 and Q3 should both be off). Follow the +2.00 volts from A2U3 pin 6, through K1, through the A5 Data Probe, back to the A2 DVM assembly A2K2, to the input of the A/D U4 pin 15.

11. Perform the Overvoltage Detector test.

    Purpose: The Overvoltage Detector circuit, consisting of U6, Q5, and assorted support circuitry, is normally a passive or nonactive circuit. The purpose of the circuit is to detect an overvoltage condition at A2R19. This point is

Table 8-10. A2 Troubleshooting Procedures (Continued)

normally 2.0 volts, generated by U3 for use during the Ohmmeter mode. If, during the Ohmmeter mode, the Data Probe tip is placed on a dc voltage, the Overvoltage Detector should sense the error and force the interrupt line OVOL low. This halts the microprocessor and the measurement, and opens the OHM Control relay, protecting the A2 DVM assembly.

Procedure:

a. To test the Overvoltage Detector circuit, place the 5005B into the OHMs (KΩ) mode.

b. Monitor OVOL, by connecting an oscilloscope or logic probe to the collector of A2Q5.

c. First, force an overvoltage condition by momentarily connecting the output of U3 pin 6 to +5 volts. The (lower) U6 Op-amp should switch states, turning Q5 on, which causes OVOL to go low.

d. Next, force an undervoltage condition, by momentarily connecting the output of U3 pin 6 to ground. The (upper) U6 Op-amp should switch states, turning Q5 on, which causes OVOL to go low.

Indications:

When either an overvoltage or undervoltage condition exists at U3 pin 6, the Overvoltage Detector should respond by driving OVOL low. Overvoltage is any dc level greater than 2.95 volts, undervoltage is any dc level less than 0.9 volts. With the overvoltage condition removed, the circuit should return to its quiescent state with OVOL high.

8-303. A3 TROUBLESHOOTING

8-304. The A3 Microprocessor Assembly contains the microprocessor, RAM, ROM, and I/O devices. A majority of the A3 circuitry is verified by the Kernel Troubleshooting Procedure in *Table 8-8*. The following diagnostics verify the Output Port and the Timer circuits.

TROUBLESHOOTING TEST	DIAGNOSTIC NUMBER
Output Port Diagnostic	0-4
Timer Diagnostic	0-5

Table 8-11. A3 Troubleshooting Procedure

1. Perform the Output Port Diagnostic (Diag 0-4).

   a. Set the diagnostic rotary switches on A3 to 0-4 (S1=0 S2=4).

   b. Connect the test signature analyzer as follows:

      Controls:

      START ..... Falling edge
      STOP ..... Rising edge
      CLOCK ..... Rising edge

      Timing Pod:

      START ..... A3 TP A15
      STOP ..... A3 TP A15
      CLOCK ..... A3 TP $\overline{RD}$
      GND ..... A3 TP GND

      NOTE

      The cable leading to the A8 HP-IB Assembly can be disconnected for convenience.

Table 8-11. A3 Troubleshooting Procedures (Continued)

c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

d. Verify the signatures for the four memory devices, U4, U8, U11, and U13 and buffers U7 and U10 as listed below:

S.A Setup — Polarities

Clk: ↓
Start: ↓
Stop: ↓

S.A. Setup — UUT Connections

Clk: $\overline{WR}$
Start/Stop: A15
Stop Qual: A15

V_{CC} Signature = F3C3

"X" Signature = Don't Care

U4

7P10	1	40	F3C3
F3C3	2	39	X
F3C3	3	38	36C6
0000	4	37	0000
F3C3	5	36	U5U5
F3C3	6	35	0000
98C9	7	34	0000
F3C3	8	33	5118
0000	9	32	H138
F3C3	10	31	0000
0000	11	30	HAH9
4357	12	29	8F6F
P22U	13	28	5CU5
01F4	14	27	5CC0
U5CC	15	26	8299
6A6F	16	25	4463
HPU4	17	24	44P0
8809	18	23	0000
H8HP	19	22	CHA3
0000	20	21	CHA3

U7

A675	1	14	F3C3
65F6	2	13	63U4
UH7H	3	12	A047
3PFP	4	11	P0CC
PF16	5	10	2308
2UA5	6	9	0000
0000	7	8	F3C3

U8

PF16	1	40	F3C3
UH7H	2	39	A675
F3C3	3	38	18UH
0000	4	37	382P
1C29	5	36	2988
F3C3	6	35	H9A8
98C9	7	34	6FA5
F3C3	8	33	U5U5
X	9	32	C058
F3C3	10	31	99H4
0000	11	30	63U4
4357	12	29	P0CC
P22U	13	28	6C5U
01F4	14	27	66A3
U5CC	15	26	C296
6A6F	16	25	H7H6
HPU4	17	24	F160
8809	18	23	6751
H8HP	19	22	8UH1
0000	20	21	82PU

U10

382P	1	14	F3C3
UC9H	2	13	H7H6
6FA5	3	12	1465
AU16	4	11	98C9
99H4	5	10	5C0A
5A67	6	9	F3C3
0000	7	8	0000

U11

251A	1	40	F3C3
F3C3	2	39	901C
F3C3	3	38	6C66
0000	4	37	31C2
F3C3	5	36	6UH7
F3C3	6	35	6PF1
98C9	7	34	0A67
F3C3	8	33	118U
0000	9	32	1382
F3C3	10	31	X
0000	11	30	X
4357	12	29	X
P22U	13	28	X
01F4	14	27	CC05
U5CC	15	26	299H
6A6F	16	25	463U
HPU4	17	24	4P0C
8809	18	23	0000
H8HP	19	22	CHA3
0000	20	21	CHA3

U13

5C0A	1	40	F3C3
F3C3	2	39	X
F3C3	3	38	X
0000	4	37	X
F3C3	5	36	X
F3C3	6	35	X
98C9	7	34	X
F3C3	8	33	X
0000	9	32	X
F3C3	10	31	F3C3
0000	11	30	F3C3
4357	12	29	F3C3
P22U	13	28	F3C3
01F4	14	27	F3C3
U5CC	15	26	F3C3
6A6F	16	25	0000
HPU4	17	24	F3C3
8809	18	23	0000
H8HP	19	22	CHA3
0000	20	21	CHA3

Indications:

This test individually checks out each of the four memory devices and their buffers. A bad signature on any memory or buffer (output) indicates a bad device.

Table 8-11. A3 Troubleshooting Procedures (Continued)

2. Perform the Timer Diagnostic (Diag 0-5).

   Purpose: The purpose of the timer diagnostic is to verify proper operation of the A3 Timer circuits.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 0-5 (S1=0 S2=5).

   b. Connect the test signature analyzer as follows:

      Controls:

      START ..... Falling edge
      STOP ..... Rising edge
      CLOCK ..... Rising edge

      Timing Pod:

      START ..... A3 TP A15
      STOP ..... A3 TP A15
      CLOCK ..... A3 TP $\overline{RD}$
      GND ..... A3 TP GND

   c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

   d. Verify the key signatures as follows:

Location	Key Signature
A3U16 pin 7	F8P6
A3U16 pin 21	0352
A3U16 pin 2	0000 (flashing)
A3U16 pin 3	0000

Indications:

The timer circuitry utilizes the divided down 10 MHz clock (2.6 MHz) and internal down-counters within U8 to generate the one-second gate interval reset to the microprocessor. If any of the signatures are incorrect, backtrace the circuit.

8-305. A4 TROUBLESHOOTING

8-306. The A4 Keyboard and Display Assembly contains the instrument display LEDs, status LEDs, and keyboard. The following diagnostics verify all LEDs and the keyboard.

TROUBLESHOOTING TEST	DIAGNOSTIC NUMBER
Display Test (Part I)	1-9
Display Test (Part II)	1-A
Keyboard Test	1-B

Table 8-12. A4 Troubleshooting Procedure

1. Perform Part I of the Display Test (Diag 1-9).

   Purpose: The purpose of Part I of the display test is to light all the front panel LEDs, allowing a visual confirmation of all front panel indicators.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 1-9 (S1=1 S2=9).

   b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

   c. Verify that all front panel LEDs, except GATE and UNSTABLE, light continuously. UNSTABLE should flash at approximately a 5 Hz rate. The MSD in the display should have only the center segment lighted.

   Indications:

   If any of the LEDs fail to light, refer to the disassembly procedures, remove the A4 assembly, and replace the LED.

2. Perform Part II of the Display Test (Diag 1-A).

   Purpose: Part II of the display test marches all the possible display characters across the display, in a repeating routine. The alarm sounds, repeating a string of 10 beeps. Additionally, the diagnostic provides signatures for the A3 Display Driver IC.

   Procedure:

   a. Set the diagnostic rotary switches on A3 to 1-A (S1=1 S2=A).

   b. Connect the test signature analyzer as follows:

      Controls:

      START ..... Falling edge
      STOP ..... Rising edge
      CLOCK ..... Rising edge

      Timing Pod:

      START ..... A3 TP A15
      STOP ..... A3 TP A15
      CLOCK ..... A3 TP $\overline{WR}$
      GND ..... A3 TP GND

   c. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

   d. Observe the display and verify that the characters listed below scroll from right to left across the rightmost five display digits.

      0.1.2.3.4.5.6.7.8.9.A.C.F.H.P.U.----

      All other remaining LEDs on the front panel should not be lighted. The diagnostic takes approximately 11 seconds to complete one cycle.

Table 8-12. A4 Troubleshooting Procedure (Continued)

e. Verify the signatures listed below, by probing the Display Decoder Driver IC, A3U6. Note that it will take at least 11 seconds to clock the data into the test signature analyzer. Hold the probe onto the lead for 2 gates to obtain accurate data.

S.A Setup — Polarities

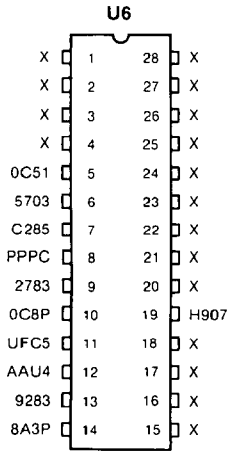
Clk: ↓
Start: ↓
Stop: ↓

S.A. Setup — UUT Connections

Clk: $\overline{WR}$
Start/Stop: A15
Stop Qual: A15

V_{CC} Signature = H907

"X" Signature = Don't Care



Indications:

If the character pattern is incorrect, or one or more of the signatures on A3U6 are incorrect, suspect A3U6.

3. Perform the Keyboard Test (Diag 1-B).

Purpose: The Keyboard test configures the instrument to respond to a keypress by the operator by displaying the corresponding front panel key number.

Procedure:

a. Set the diagnostic rotary switches on A3 to 1-B (S1=1 S2=B).

b. Turn the UUT LINE switch from ON to OFF then back to ON. This initiates the diagnostic.

Table 8-12. A4 Troubleshooting Procedure (Continued)

c. In any sequence, press each of the front panel keys during the time that the display shows --19 and the alarm is sounding. Verify that the display responds with key codes as listed below:

KEY	DISPLAY
NORM	16 GATE UNSTABLE
QUAL	17 GATE UNSTABLE
kHz	05 GATE UNSTABLE
TOTLZ	13 GATE UNSTABLE
ms	09 GATE UNSTABLE
kΩ	01 GATE UNSTABLE
DCV	04 GATE UNSTABLE
V	12 GATE UNSTABLE
Vp+	08 GATE UNSTABLE
Vp-	00 GATE UNSTABLE

KEY	DISPLAY
DATA	02 GATE UNSTABLE
CLOCK	14 GATE UNSTABLE
ST-TP-QL	10 GATE UNSTABLE
⇧	18 GATE UNSTABLE
⇩	06 GATE UNSTABLE
CLOCK	03 GATE UNSTABLE
START	15 GATE UNSTABLE
STOP	11 GATE UNSTABLE
QUAL	07 GATE UNSTABLE

Indications:

If any one of the key responses are incorrect, suspect the corresponding pushbutton key. If several key responses are incorrect, check for a shorted or open trace or bad ribbon cable wire in the X and Y matrix lines from A3U3 or A8U20. If all the key responses are incorrect, suspect A3U3 or A8U20.

8-307. A8 TROUBLESHOOTING

8-308. The A8 HP-IB Assembly contains all the circuitry necessary to monitor 5005B operation and provide external keypress capability from a controller. The following procedure tests critical areas of the assembly.

Table 8-13. A8 Troubleshooting

Test for proper signatures on the HP-IB Assembly.

Purpose: The purpose of this procedure is to verify key sigantures on the A8 Assembly.

Procedure:

a. Remove the jumper W1-W9 from the A8 Assembly.

b. Connect the test signature analyzer as follows:

Controls:

START ..... Rising edge
STOP ..... Rising edge
CLOCK ..... Rising edge

Timing Pod:

START ..... A8 TP A15
STOP ..... A8 TP A15
CLOCK ..... A8 TP $\overline{RD}$
GND ..... A8 TP GND

c. Turn the UUT LINE switch fron ON to OFF then back to ON. This initiates the freerun condition of the HP-IB microprocessor.

d. Verify the signatures listed below by probing U5, U7, U8, U15, U21, and U22.

S.A Setup — Polarities

Clk: ⨍
Start: ⨍
Stop: ⨍

S.A. Setup — UUT Connections

Clk: RD
Start/Stop: A15
Stop Qual: A15

V_{CC} Signature = 0001

"X" Signature = Don't Care

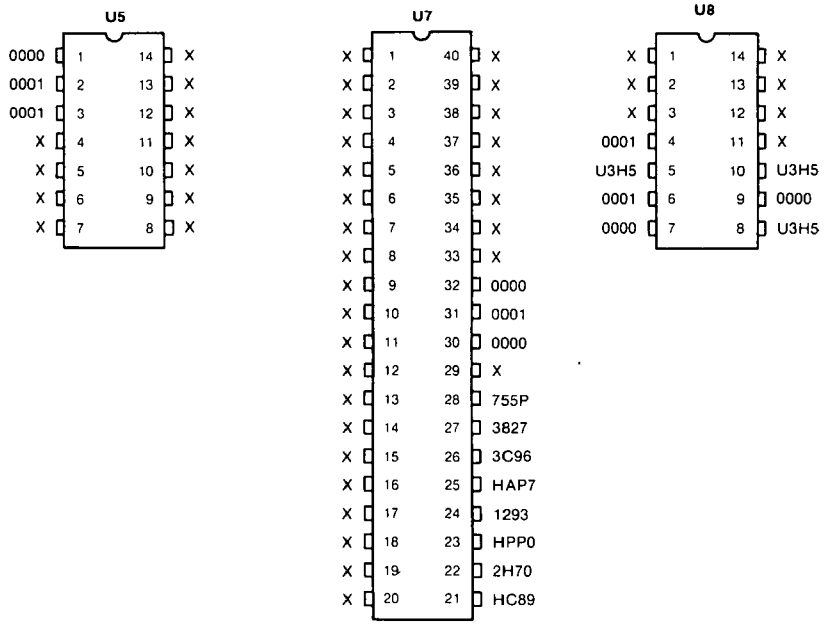
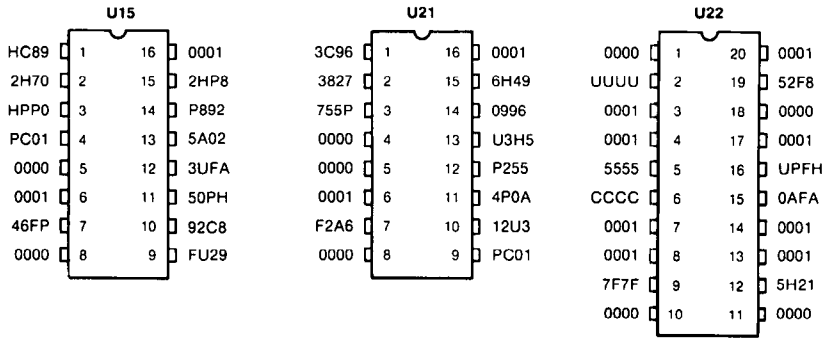


Table 8-13. A8 Troubleshooting (Continued)



Indications:

This test individually checks out key signatures on the HP-IB Assembly. Any bad signatures on any IC should be backtraced to its source to find the faulty part.

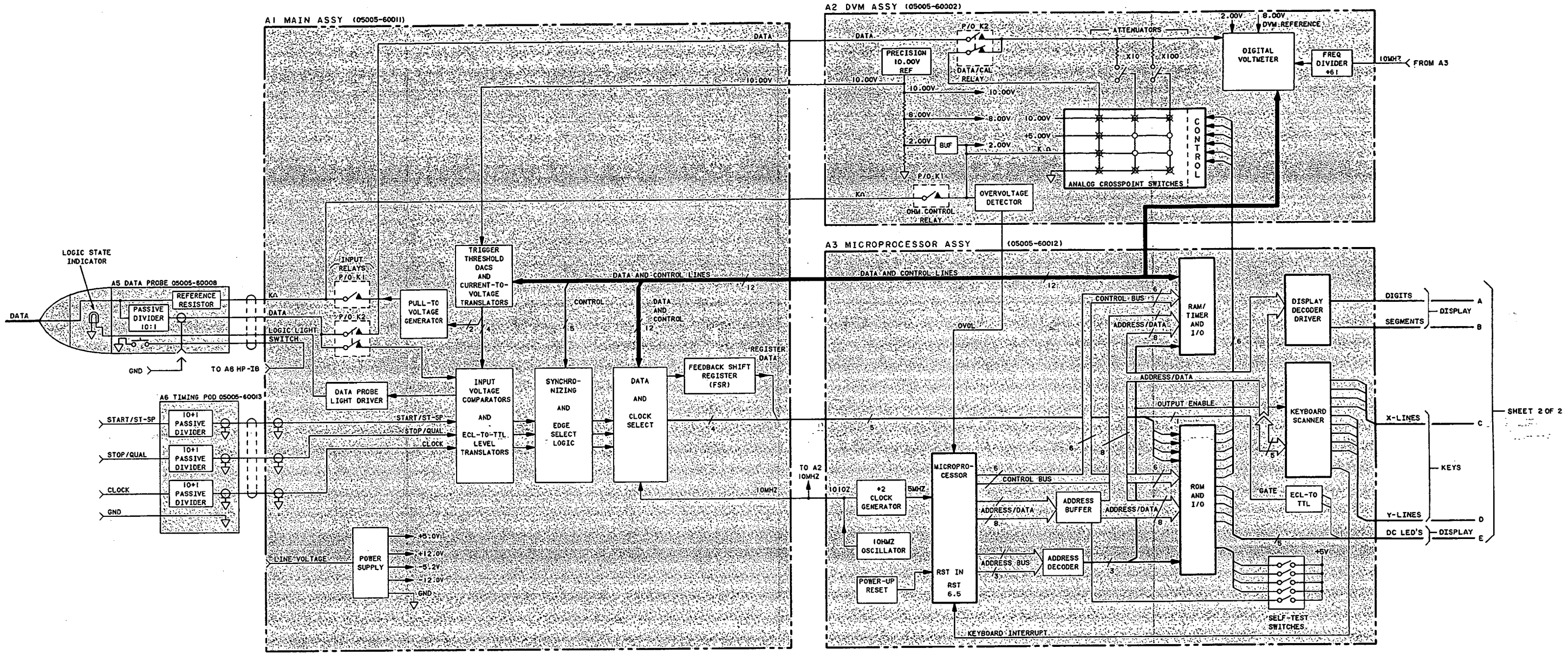


Figure 8-18. Block Diagram (Sheet 1 of 2)

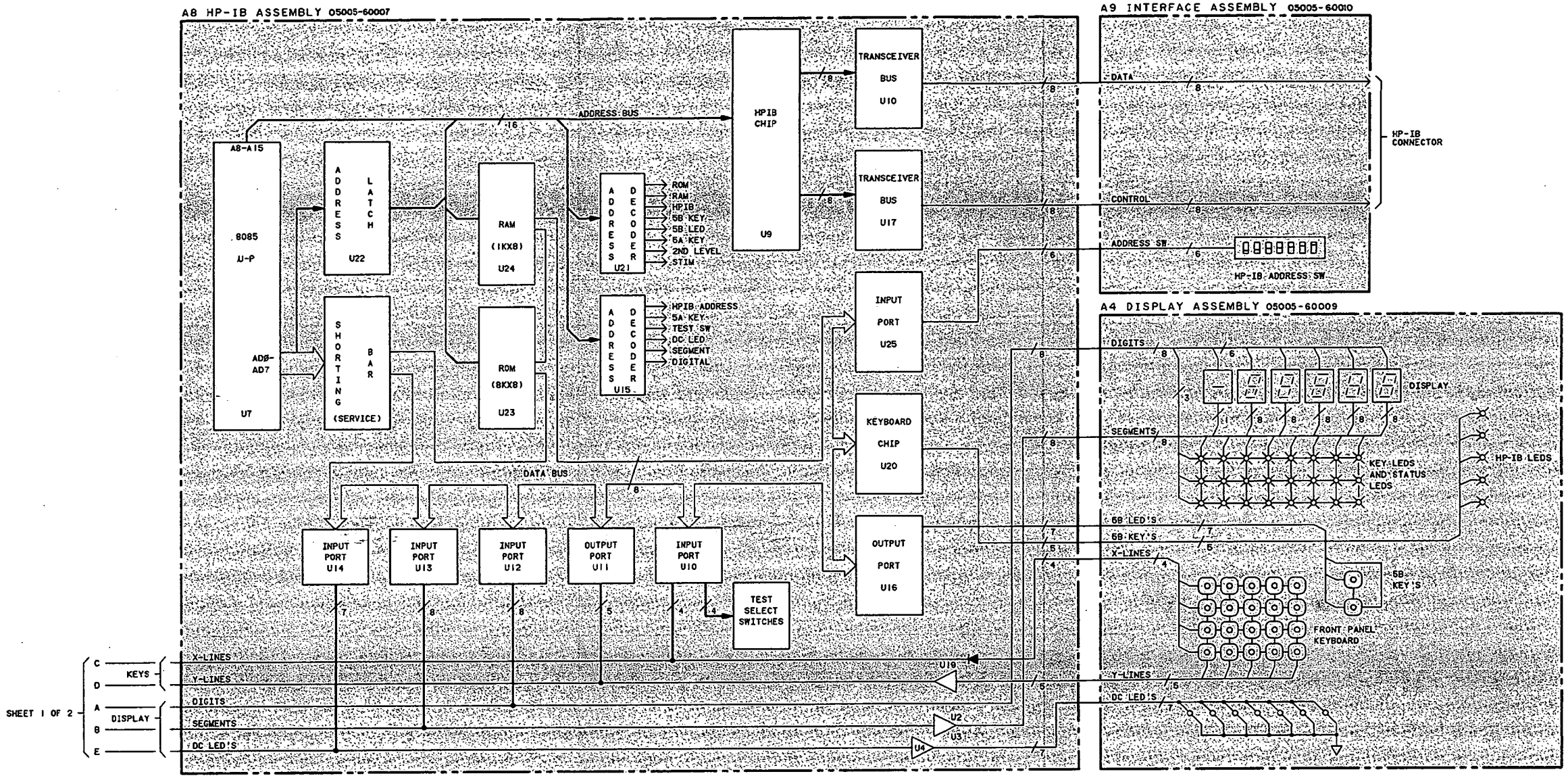
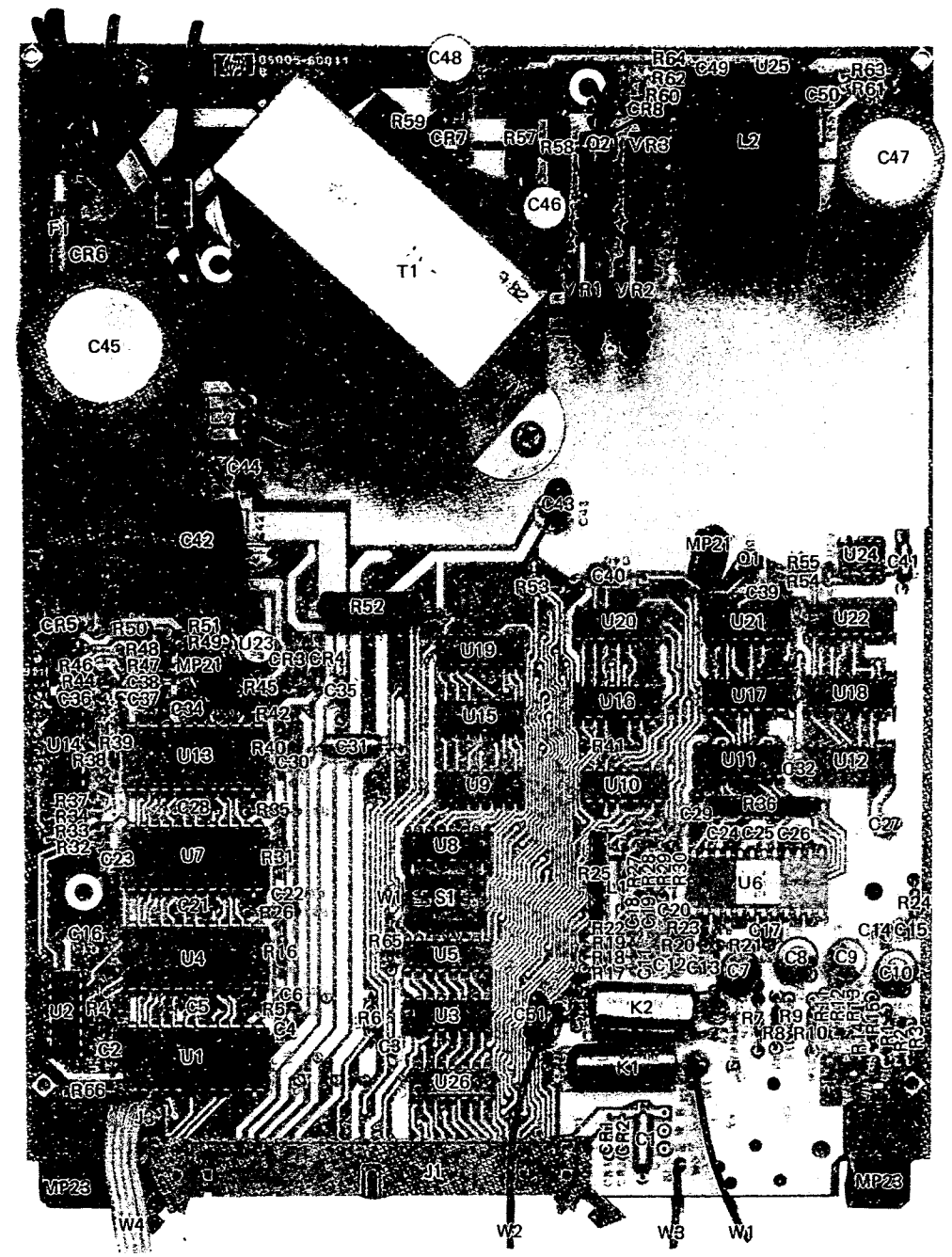


Figure 8-18. Block Diagram (Sheet 2 of 2)

Figure 8-18
BLOCK DIAGRAM
(Sheet 1 of 2)

(See Page 8-97)



A1/A7

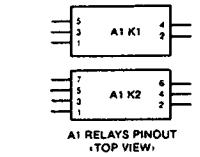
Figure 8-18
BLOCK DIAGRAM
(Sheet 2 of 2)

(See Page 8-99)

NOTES

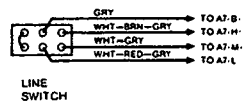
A1J1 CONNECTOR PINOUT
CIRCUIT SIDE OF BOARD

	TP4	35	30	END OF MEASURE	
	TP3	34	29	LSB COUNT	
	DATA (PROBE)	33	28	REGISTER DATA	
	GATE	32	27	POLARITY DIFF	TD0
	TD1	31	26	SYNC	
TD2	START EDGE	30	25	CLOCK EDGE	DA0
SIGN	COMBINED STOP/START	29	24	START MEASURE	
DA1	STOP/DUAL EDGE	28	23	POP	
	OUTPUT SHIFT ENABLE	27	22	SIGNATURE-TI	TD4
TD3	DATA STROBE	26	21	FREQ-SIGN	POP
TD5	COUNT	25	20	DSTR	
	DUAL ENABLE	24	19	+5V	TD7
	+5V	23	18	+5V	
	GND	22	17	GND	
	10 MHz	21	16	GND	
	N.C.	20	15	GND	
	N.C.	19	14	+10.00V	
	N.C.	18	13	N.C.	
	N.C.	17	12	N.C.	
	N.C.	16	11	N.C.	
	N.C.	15	10	N.C.	
	N.C.	14	9	+12V	
	N.C.	13	8	GND (A)	
	N.C.	12	7	-12V	
	N.C.	11	6	GND (D)	
	N.C.	10	5	-5V	
	N.C.	9	4	-5.2V	
	N.C.	8	3	N.C.	
	N.C.	7	2	N.C.	
	N.C.	6	1	N.C.	



A1 RELAYS PINOUT
(TOP VIEW)

W2 (HP PART #05005-60101)



LINE
SWITCH

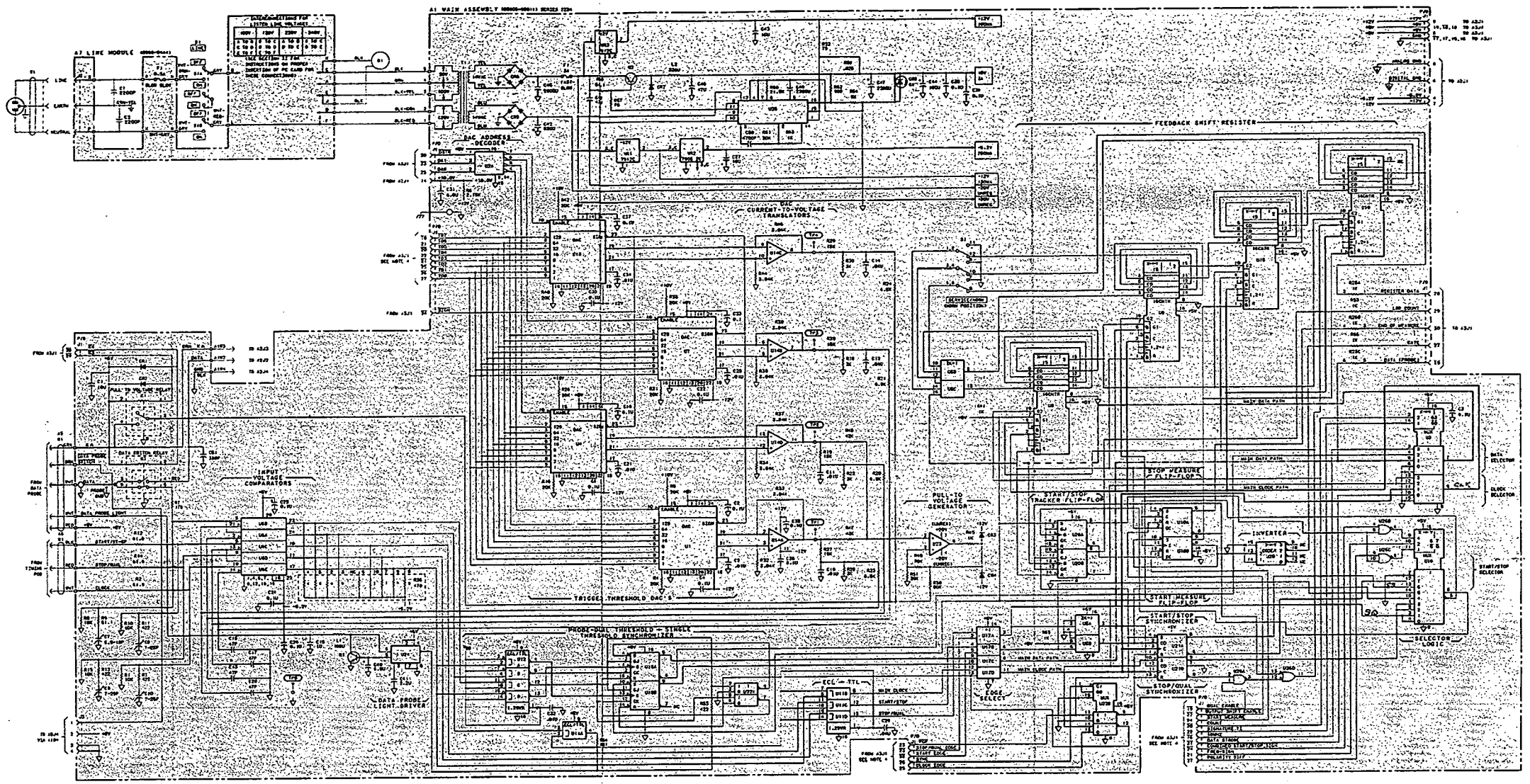
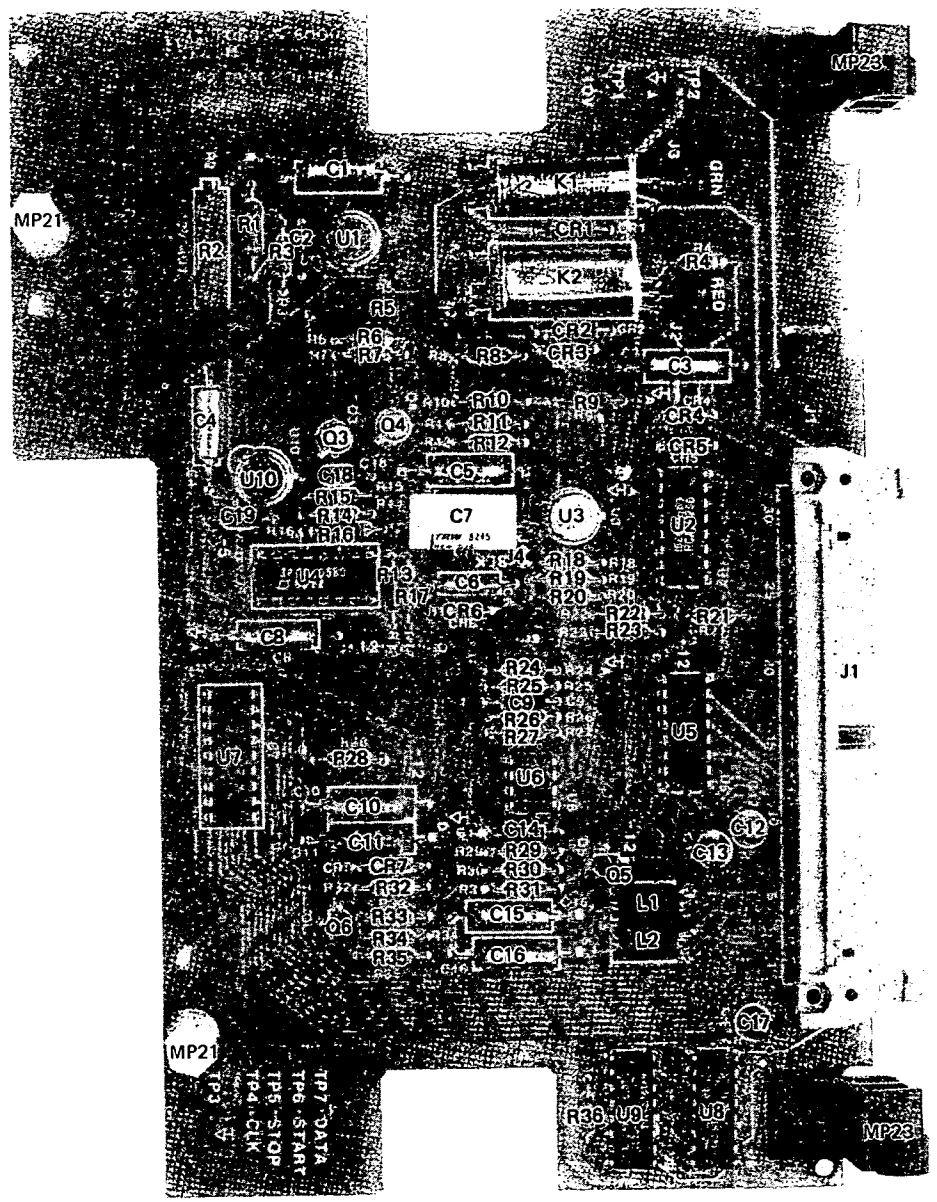


Figure 8-19. A1/A7 Main Assembly Schematic Diagram



A2

Figure 8-19
A1 MAIN/A7 POWER MODULE ASSEMBLY DIAGRAM

(See Page 8-101)

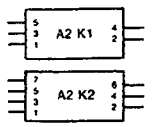
NOTES

A2J1 CONNECTOR PINOUT
CIRCUIT SIDE OF BOARD

N.C.	30	30	N.C.
N.C.	29	29	N.C.
N.C.	28	28	N.C.
N.C.	27	27	N.C.
N.C.	26	26	N.C.
N.C.	25	25	N.C.
N.C.	24	24	N.C.
N.C.	23	23	N.C.
N.C.	22	22	N.C.
N.C.	21	21	N.C.
N.C.	20	20	N.C.
N.C.	19	19	N.C.
+5V	18	18	N.C.
N.C.	17	17	N.C.
10 MHz	16	16	N.C.
K2	15	15	GND
K1	14	14	+10.00V
C	13	13	D
B	12	12	SW
RESET	11	11	A
D4	10	10	STROBE
D3	9	9	+12V
D5	8	8	GND ‹A›
DV SIGN	7	7	-12V
B3	6	6	GND ‹D›
B2	5	5	+5V
B0	4	4	-5.2V
M/Z	3	3	START
D2	2	2	D1 ‹LSD›
OVOL	1	1	B1

∇_A = ANALOG GROUND

∇ = DIGITAL GROUND



A2 RELAYS PINOUT
TOP VIEW

Troubleshooting:

The following troubleshooting procedures are provided to verify the proper operation, and isolate malfunctioning components on the A2 DVM Assembly. Procedures begin with paragraph 8-300.

Troubleshooting Test	Diagnostic Number
Test Point Measurements	—
Zero Offset Value / 25V range	1-0
Zero Offset Value / 250 V range	1-3
Auto-Calibration / 25 V range	1-4
Uncorrected Reading / 25 V range	1-2
Uncorrected Reading / 250 V range	1-5
Zero Offset Value / Ohms Mode	1-6
Reference Voltage / Ohms Mode	1-7
Measured Voltage / Ohms Mode	1-8
Overvoltage Detector Test	—

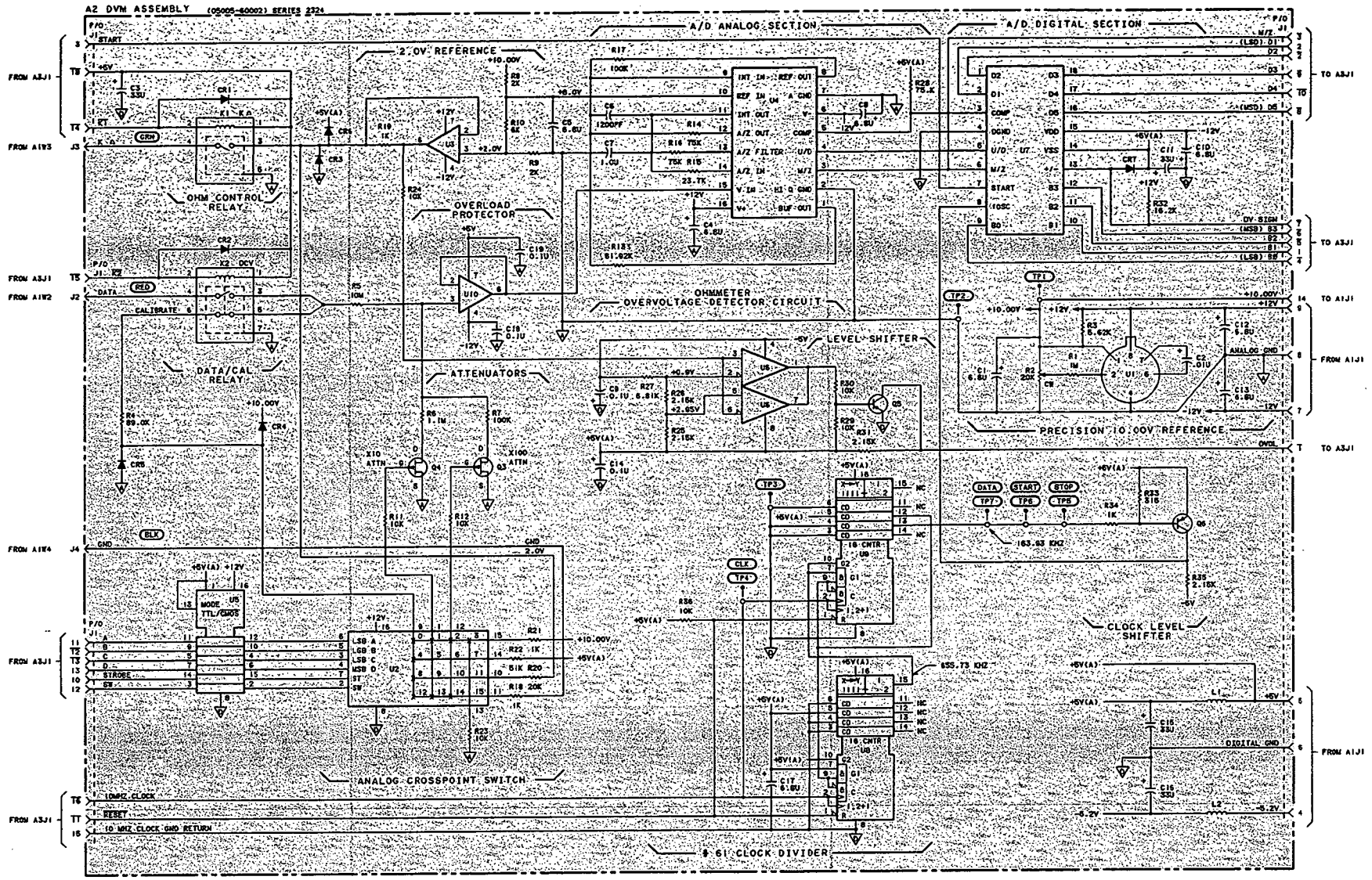
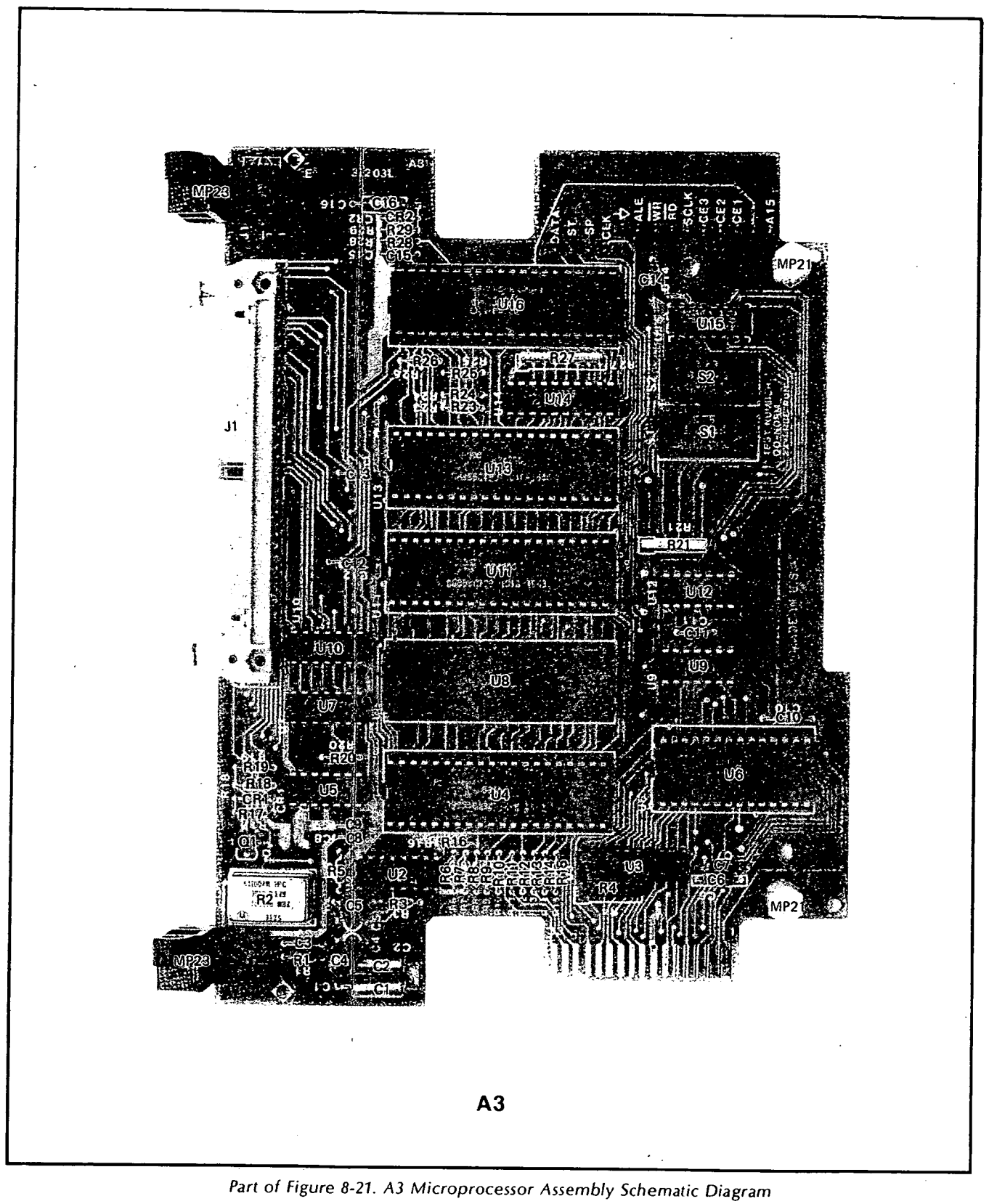


Figure 8-20. A2 DVM Assembly Schematic Diagram



A3

Part of Figure 8-21. A3 Microprocessor Assembly Schematic Diagram

Figure 8-20
A2 DVM ASSEMBLY SCHEMATIC DIAGRAM

(See Page 8-103)

NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR A COMPLETE REFERENCE DESIGNATION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS
   CAPACITANCE IN FARADS
   INDUCTANCE IN HENRIES
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT VALUE. AVERAGE VALUE SHOWN.

A3 REFERENCE DESIGNATORS

A3C1-C16
A3CR1, CR2
A3J1
A3Q1
A3R1-R21, ,R23-R29
A3R22 Not Used
A3S1, S2
A3U1-U16

A3 ACTIVE COMPONENTS

REFERENCE	HP PART NO.
A3CR1	1901-0518
A3CR2	1901-0040
A3Q1	1854-0215
A3U1	1813-0139
A3U2	1820-1052
A3U3	1820-2309
A3U4	1818-1542
A3U5, U12	1820-1112
A3U6	1820-2132
A3U7, U10	1820-0174
A3U8	1818-0696
A3U9	1818-1208
A3U11	1820-1543
A3U13	1818-1544
A3U14	1820-2075
A3U15	1820-1245
A3U16	1820-2074

A3J1 CONNECTOR PINOUT CIRCUIT SIDE OF BOARD

	$\overline{K4}$	30	30	END OF MEASURE	
	$\overline{K3}$	29	29	LSB COUNT	
DATA (PROBE)		28	28	REGISTER DATA	
GATE		27	27	POLARITY DIFF	--TD0
TD1		26	26	SYNC	
--TD2	START EDGE		25	CLOCK EDGE	--DA0
--SIGN	$\overline{\text{COMBINED STOP/START}}$		24	$\overline{\text{START MEASURE}}$	
--DA1	STOP/QUAL EDGE		23	$\overline{\text{POP}}$	
	$\overline{\text{OUTPUT SHIFT ENABLE}}$		22	SIGNATURE-TI	--TD4
--TD3	DATA STROBE		21	FREQ-SIGN	--$\overline{\text{POP}}$
--TD5	COUNT		20	$\overline{\text{DSTR}}$	
	QUAL ENABLE		19	+5V	--TD7
	+5V		18	+5V	
	GND		17	GND	
	10 MHz		16	GND	
	N.C.		15	GND	
	$\overline{K1}$		14	N.C.	
	C		13	D	
	B		12	SW	
	N.C.		11	A	
	D4		10	STROBE	
	D3		9	N.C.	
	D5		8	N.C.	
	DV SIGN		7	N.C.	
	B3		6	N.C.	
	B2		5	N.C.	
	B0		4	-5.2V	
	M/Z		3	START	
	D2		2	D1 (LSD)	
	OVOL		1	B1	

A3J2 CONNECTOR PINOUT CIRCUIT SIDE OF BOARD

34	a
33	b
32	f
31	GATE LIGHT
30	DEVICE ENABLE 2
29	UNCAL
28	UNSTABLE
27	CLOCK EDGE
26	CLOCK EDGE
25	Y2
24	X2
23	Y3
22	DEVICE ENABLE 4
21	Y4
20	X4
19	Y5
18	g
17	c
16	+5V
15	+5V
14	e
13	d
12	ST EDGE
11	ST EDGE
10	X1
9	Y1
8	DEVICE ENABLE 5
7	DEVICE ENABLE 7
6	dp
5	X3
4	DEVICE ENABLE 3
3	DEVICE ENABLE 0
2	DEVICE ENABLE 1
1	DEVICE ENABLE 6

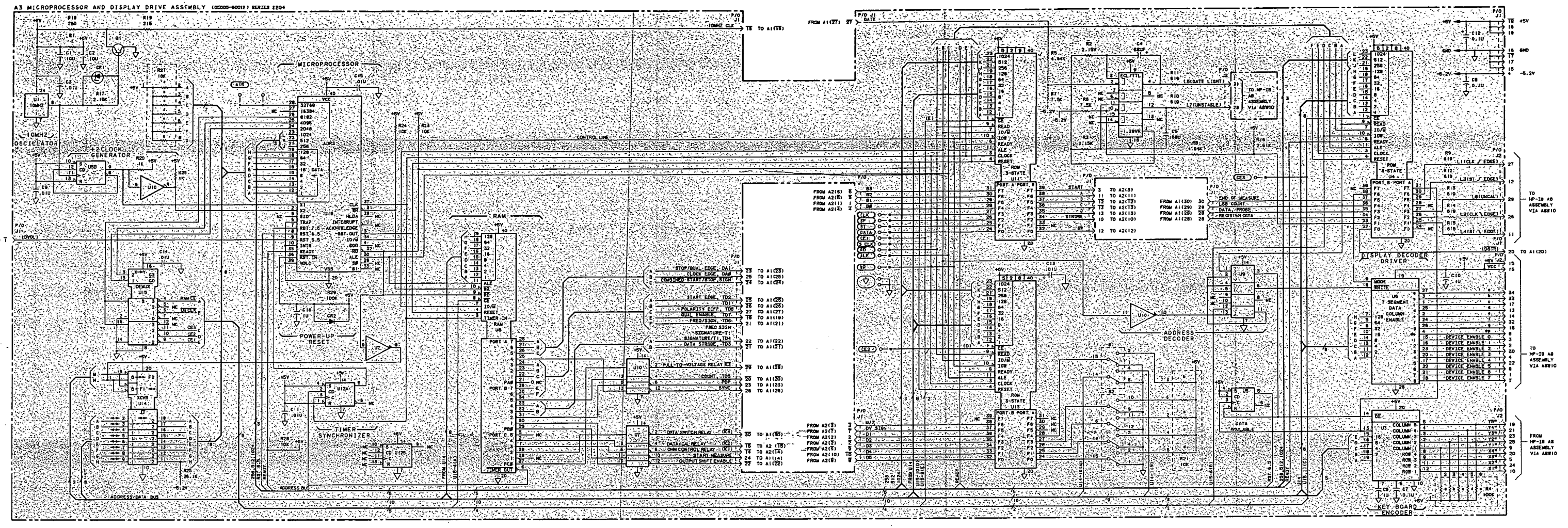


Figure 8-21. A3 Microprocessor Assembly Schematic Diagram

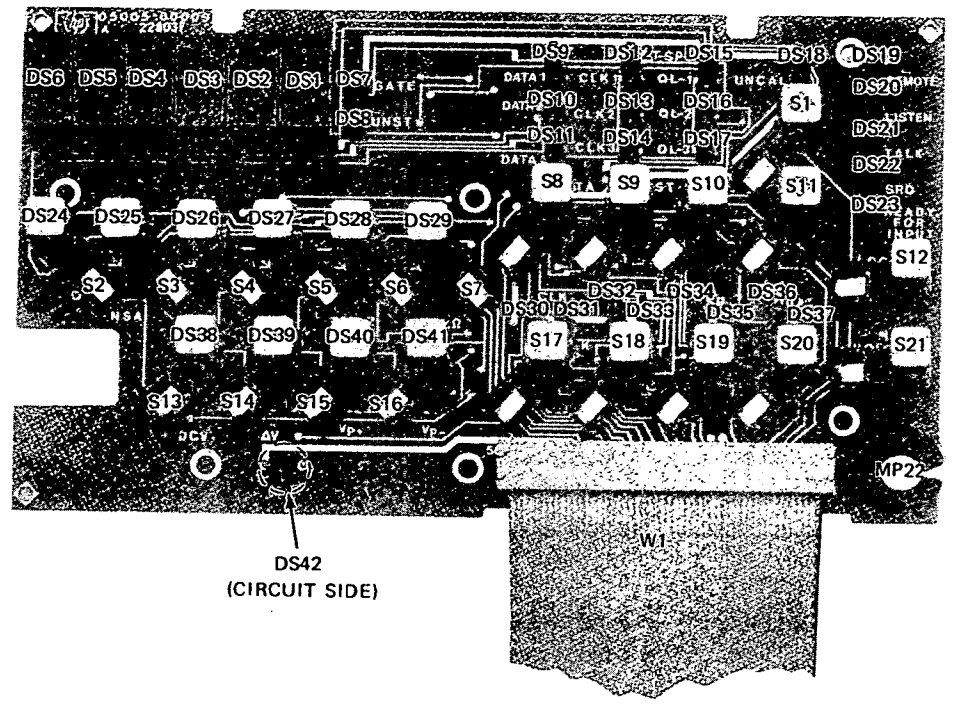
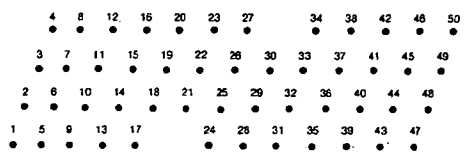


Figure 8-21
A3 MICROPROCESSOR ASSEMBLY SCHEMATIC DIAGRAM

(See Page 8-105)

NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR A COMPLETE REFERENCE DESIGNATION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS
   CAPACITANCE IN FARADS
   INDUCTANCE IN HENRIES
3. A4W1 CONNECTIONS TO A4 (CIRCUIT SIDE) ARE AS FOLLOWS:



A4 REFERENCE DESIGNATORS

A4DS1-DS42
A4S1, S2
A4W1

A4 ACTIVE COMPONENTS

REFERENCE	HP PART NO.
A4DS1-DS6	1990-0730
A4DS7-DS22, DS30-DS37	1990-0547
A4DS23	1990-0487
A4DS24-DS29, DS38-DS41	1990-0685
A4DS42	0960-0553
A4S1-S21	5060-9436

NOTES

A4W1 CONNECTOR PINOUT CIRCUIT SIDE OF BOARD

34 a
33 b
32 f
31 GATE LIGHT
30 DEVICE ENABLE 2
29 UNCAL
28 UNSTABLE
27 CLOCK EDGE
26 CLOCK EDGE
25 Y2
24 X2
23 Y3
22 DEVICE ENABLE 4
21 Y4
20 X4
19 Y5
18 g
17 c
16 +5V
15 -5V
14 e
13 d
12 ST EDGE
11 ST EDGE
10 X1
9 Y1
8 DEVICE ENABLE 5
7 DEVICE ENABLE 7
6 dp
5 X3
4 DEVICE ENABLE 3
3 DEVICE ENABLE 0
2 DEVICE ENABLE 1
1 DEVICE ENABLE 6

Troubleshooting:

The following troubleshooting procedures are provided to verify the proper operation, and isolate malfunctioning components on the A4 Display Assembly. Procedures begin with paragraph 8-305.

Troubleshooting Test	Diagnostic Number
Display Test (Part I)	1-9
Display Test (Part II)	1-A
Keyboard Test	1-B

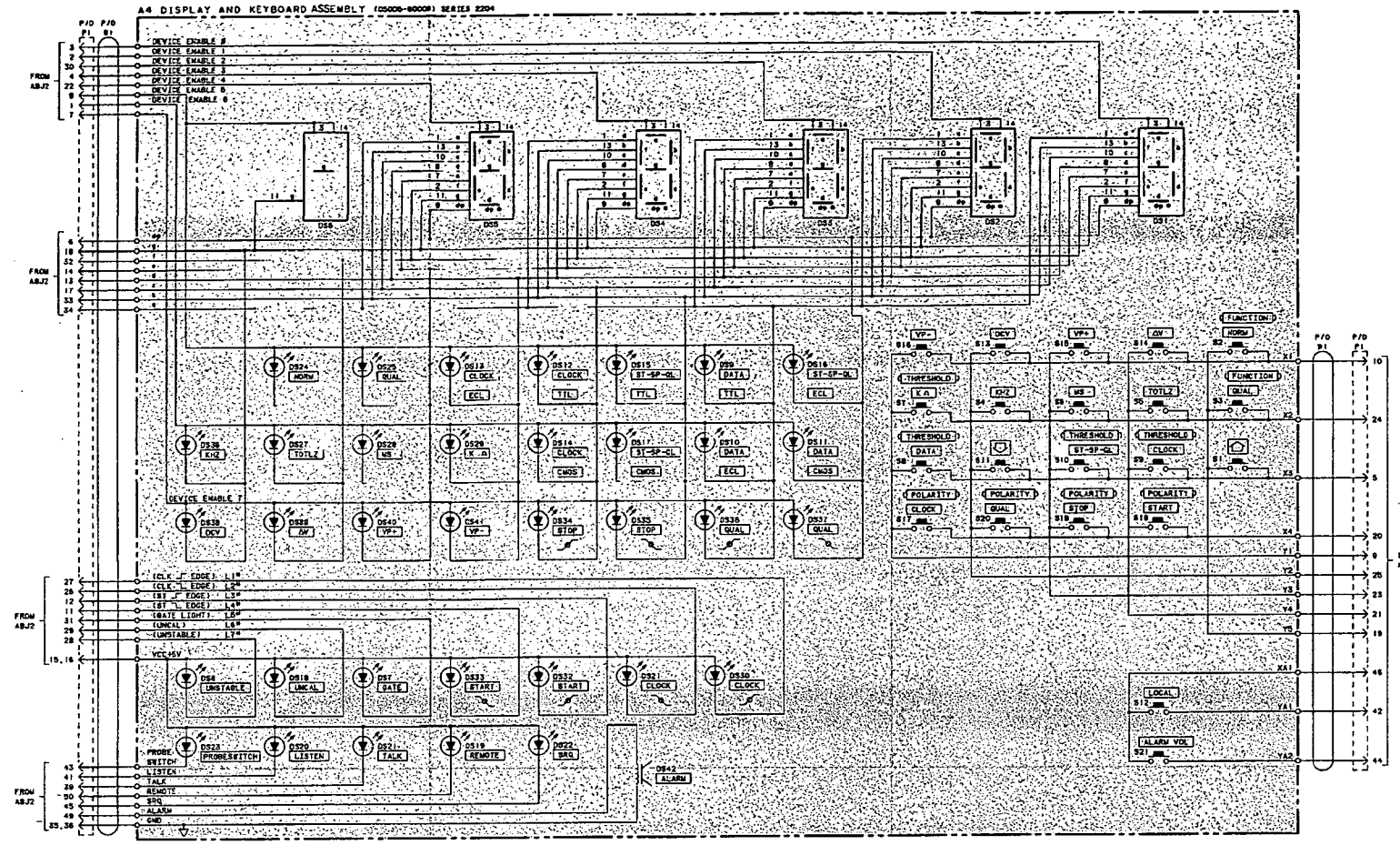
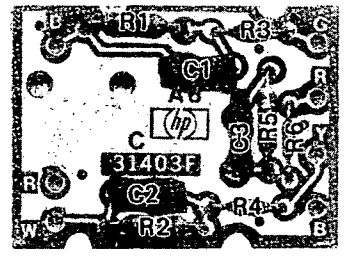


Figure 8-22. A4 Display and Keyboard Assembly Schematic Diagram

A5



A6

Figure 8-22
A4 DISPLAY AND KEYBOARD ASSEMBLY DIAGRAM

(See Page 8-107)

NOTES

A5

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR A COMPLETE REFERENCE DESIGNATION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS
   CAPACITANCE IN FARADS
   INDUCTANCE IN HENRIES
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT VALUE. AVERAGE VALUE SHOWN.
4. COAXIAL GROUND IS CONNECTOR TO A1 COAXIAL GROUND.

A5
REFERENCE
DESIGNATORS

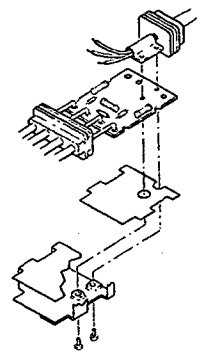
A5C1 A5DS1 A5R1, R2

A5 ACTIVE COMPONENTS

REFERENCE	HP PART NO.
A5DS1	2140-0346

A6

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR A COMPLETE REFERENCE DESIGNATION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS
   CAPACITANCE IN FARADS
   INDUCTANCE IN HENRIES
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT VALUE. AVERAGE VALUE SHOWN.
4. THE PLACEMENT OF THE METAL SHIELD WITHIN THE POD IS AS FOLLOWS:

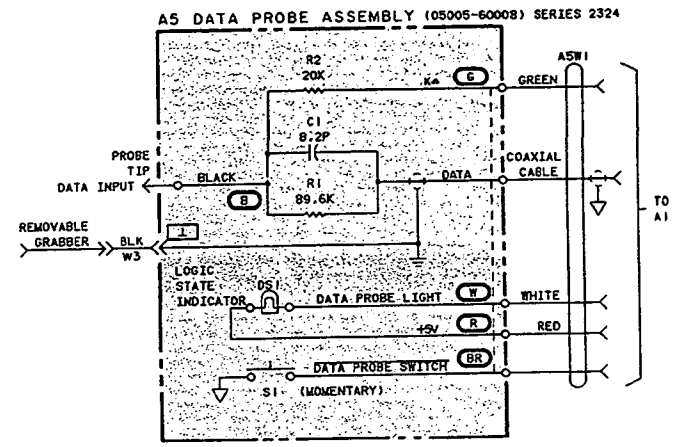


A6
REFERENCE
DESIGNATORS

A6C1-C3 A6R1-R6

A6 ACTIVE COMPONENTS

REFERENCE	HP PART NO.
NONE	



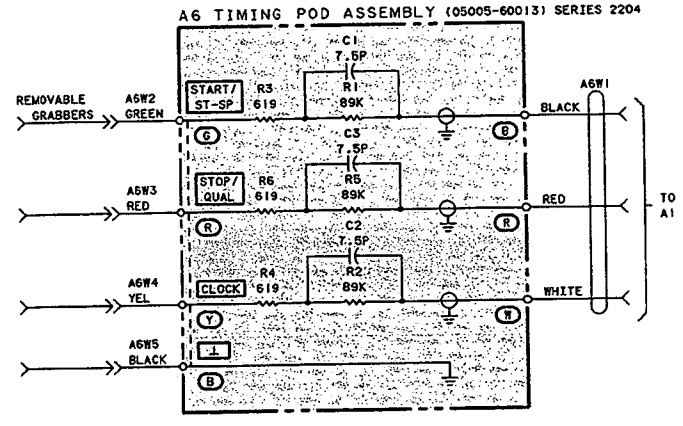


Figure 8-23. A5 Data Probe/A6 Timing Pod Assembly Schematic Diagram

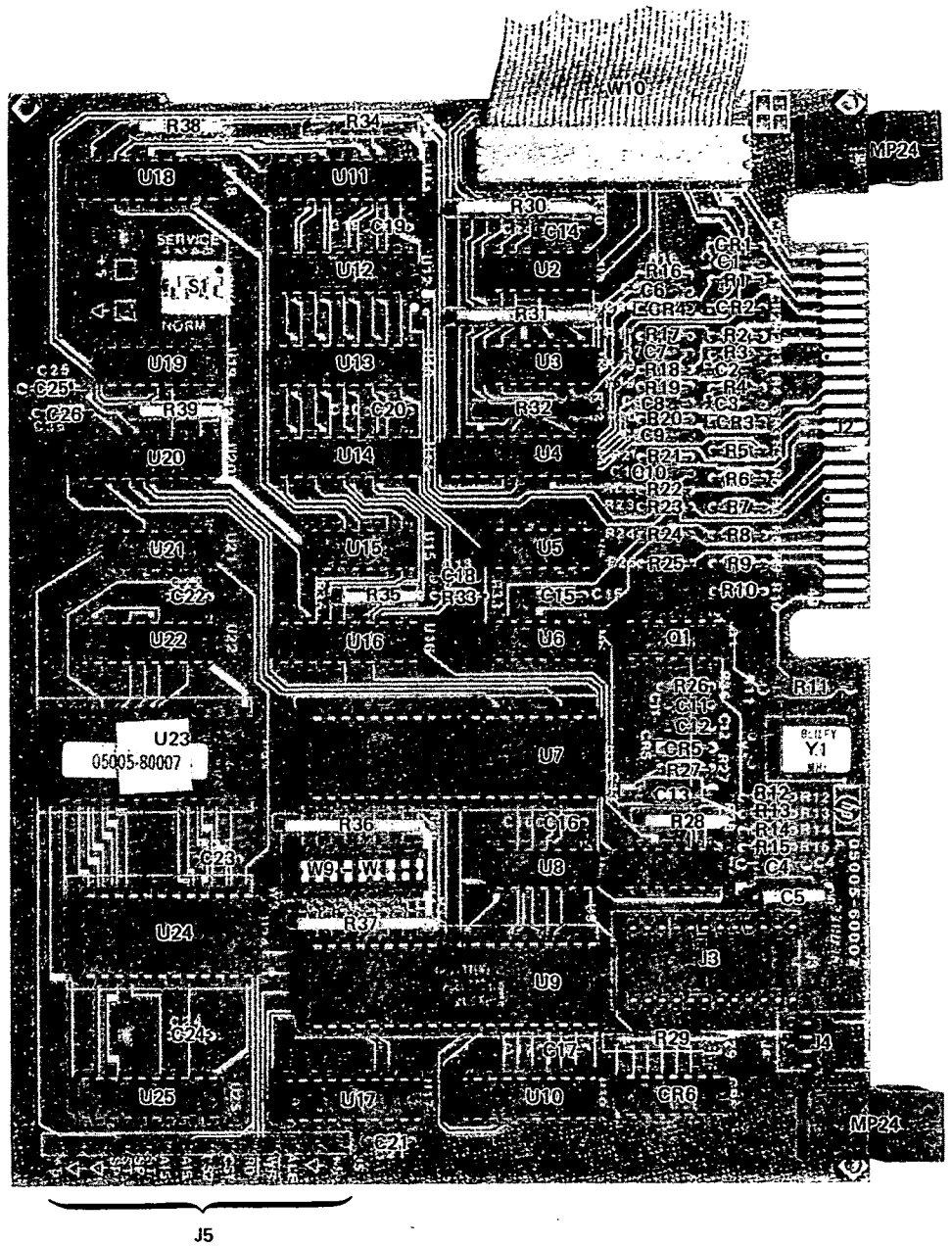
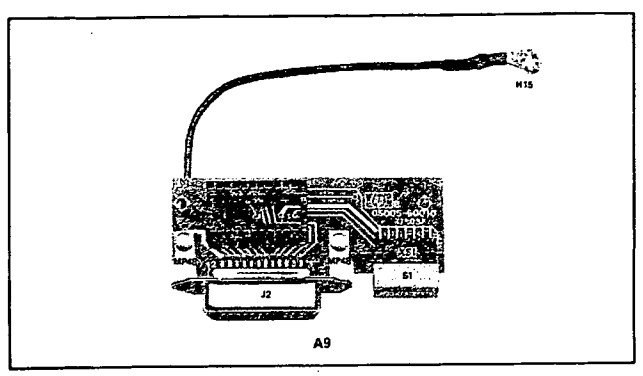


Figure 8-23
A5 DATA PROBE/
A6 TIMING POD ASSEMBLY SCHEMATIC DIAGRAM

(See Page 8-109)



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR A COMPLETE REFERENCE DESIGNATION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS
   CAPACITANCE IN FARADS
   INDUCTANCE IN HENRIES

A8 REFERENCE DESIGNATORS

A8C1-C26
A8CR1-CR8
A8J2-J5
A8Q1
A8R1-R39
A8S1
A8TP1, TP2
A8U1-U25
A8W1-W10
A8Y1
A8J1 Not Used

A8 ACTIVE COMPONENTS

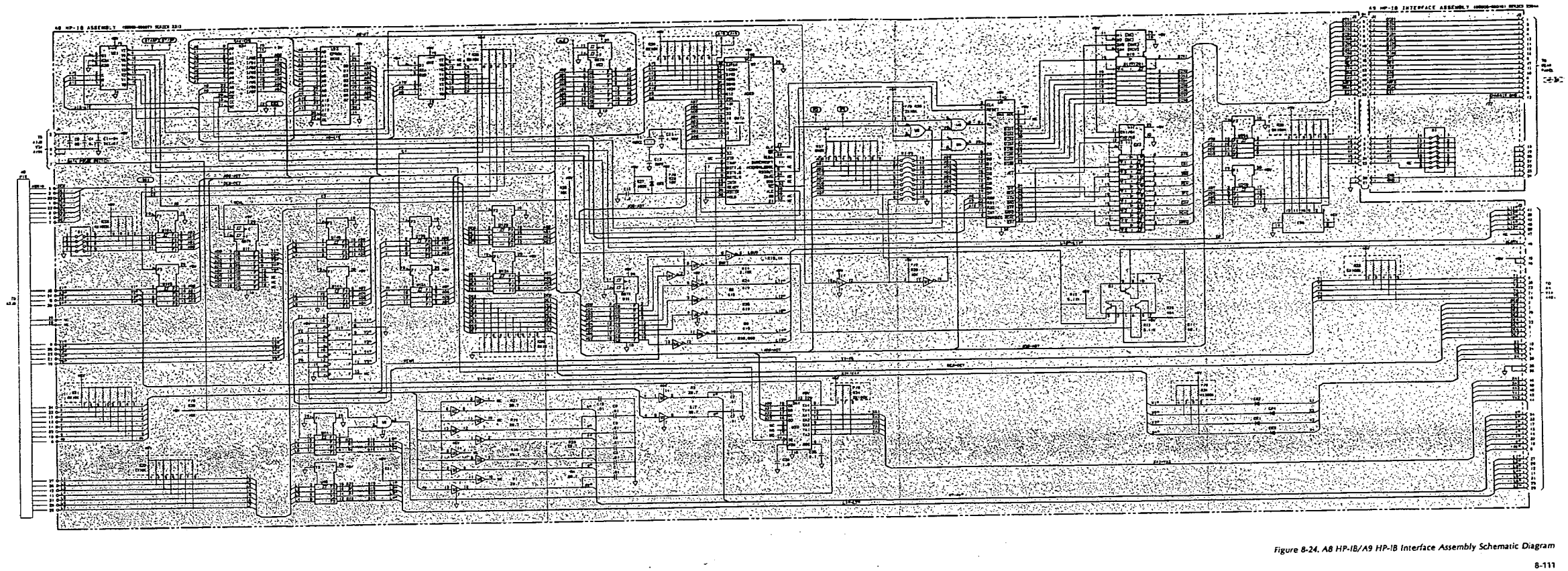
REFERENCE	HP PART NO.
A8CR1-CR5	1901-0050
A8CR6	1908-0229
A8D1	1838-0010
A8J1	1820-1200
A8J2, U3	1820-0618
A8J4,U13,U14,U18,U25	1820-2537
A8J5	1820-1197
A8J6	1820-1199
A8J7	1820-2074
A8J8	1820-1208
A8J9	1820-2549
A8J10	1820-2465
A8J11, U16	1820-2216
A8J12	1820-2024
A8J15, U21	1820-1216
A8J17	1820-2483
A8J19	1820-1256
A8J20	1820-2309
A8J22	1820-2102
A8J23	1818-3161
A8J24	1818-1967

A9 REFERENCE DESIGNATORS

A9J1, J2
A9S1

A9 ACTIVE COMPONENTS

REFERENCE	HP PART NO.
NONE	



Troubleshooting:

The troubleshooting procedures for the A8 Assembly begins with paragraph 8-307.

Figure 8-24. A8 HP-IB/A9 HP-IB Interface Assembly Schematic Diagram

Figure 8-24

A8 HP-IB/A9 HP-IB INTERFACE ASSEMBLY SCHEMATIC DIAGRAM

(See Page 8-111)

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Arranged alphabetically by country

Product Line Sales/Support Key

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C	Computer Systems Sales only
CH	Computer Systems Hardware Sales and Services
CS	Computer Systems Software Sales and Services
E	Electronic Instruments & Measurement Systems
M	Medical Products
MP	Medical Products Primary SRO
MS	Medical Products Secondary SRO
P	Personal Computation Products
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March 1983 5952-6900

HP distributors are printed in italics.

MANUAL PART NUMBER 05005-90015

PRINTED IN U.S.A.

*** * * * MANUAL UPDATING COVERAGE* * * ***

This supplement adapts your manual to instruments with serial numbers prefixed through **2510.**

*** * * * MANUAL IDENTIFICATION * * * ***

Instrument: HP 5005B
SIGNATURE MULTIMETER
OPERATING & SERVICE
MANUAL

Manual Part No: 05005-90015
Manual Microfiche: 05005-90016
Manual Print Date: SEPT 1983

ABOUT THIS SUPPLEMENT

The information in this supplement is provided to correct manual errors and to adapt the manual to instruments containing changes after the manual print date.

Change and correction information in this supplement is itemized by page numbers corresponding to the original manual pages. The pages in this supplement are organized in numerical order by manual page number.

Manual updating supplements are revised as often as necessary to keep manuals as accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of this supplement. Free copies are available from all HP offices. When requesting copies quote the model number, print date, and part number listed at the top of this page.

HOW TO USE THIS SUPPLEMENT

Insert this title page in front of the title page in your manual.

Perform all changes specified for "All Serials", and all changes through the Series Prefix of your instrument or board.

Insert any complete replacement pages provided into your manual in the proper location.

If your manual has been updated according to the last edition of this supplement, you need only perform those changes pertaining to the new series prefix. See List of Effective Pages on the reverse side of this page. New information affecting "All Serials" will be indicated by a "#" in front of the page number.

LIST OF EFFECTIVE PAGES

SERIAL PREFIX OR SERIAL NUMBER	PAGES
All Serials	xii, 6-9, 6-25
2342A	6-14, 6-16, 8-103
2414A	6-24, 8-111
2438A	6-14, 8-101
2510A	6-30

SERIAL PREFIX OR SERIES NUMBER	CHANGES

Page xii. Safety Considerations:

All Serials >Add page xii, Safety Considerations, included in these manual changes.

Page 6-9, Figure 6-4. Cabinet Parts & Hardware (Rear Panel):

All Serials >Change A9J2 from 1251-3283 to 1252-0324 CONN, 24-PIN.

Page 6-14, Table 6-2. A1 Main Assembly Replaceable Parts:

2342A >Change U18, U20 from 1820-0629 to 1820-2992 IC-FF TTL S J-K NEG-EDGE TRIG.

2438A >Change A1 (05005-60011) SERIES to 2438.
>Add XU1, XU4, XU7, XU13 1200-0541 IC-SOCKET 24-PIN.

Page 6-16, Table 6-2. A2 DVM Assembly Replaceable Parts:

2342A >Change A2 (05005-60002) SERIES to 2342.
>Add R38, R38 0698-7288 RESISTOR 147K 1% .05W F TC=0+-100.
>Add 0360-0124 CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND.
>Add XU4 1200-0607 SOCKET-IC 16-CONT DIP DIP-SLDR.

Pages 6-23/6-24, Table 6-2. A8 HP-IB Assembly Replaceable Parts:

2414A >Change A8 (05005-60007) SERIES to 2414.
>Change A8U10 from 1820-2485 to 1820-3431.

Page 6-25, Table 6-2. A9 (05005-60010) HP-IB Interface Replacement Parts:

All Serials >Change A9J2 from 1251-3283 to 1252-0324 CONNECTOR, 24-PIN.

SERIAL PREFIX OR SERIES NUMBER	CHANGES

Page 6-26, Table 6-2. Miscellaneous/Chassis Parts:

2510A

>Change MP1 from 5020-8815 to 5021-5815 FRAME-FRONT, METRIC.
>Change MP2 from 5020-8836 to 5021-5836 STRUT, METRIC.
>Change MP3 from 5020-8816 to 5021-5816 FRAME-REAR, METRIC.
>Change MP7 from 5040-7219 to 5021-6819 STRAP HNDL CAP-FRONT.
>Change MP8 from 5040-6820 to 5041-6820 STRAP HNDL CAP-REAR.
>Change MP10 from 5060-9964 to 5061-9564 COVER-BOTTOM, METRIC.
>Add 0515-1055 SCREW-MACH M4 X 0.7 6MM LG.
>Add 0515-1132 SCREW-MACH M5 X 0.8 10MM LG.
>Add 0515-1331 SCREW-MACH M4 X 0.7.
>Add 0535-0081 NUT-HEX M5 X 0.8.

NOTE

This changes 5005B cabinet parts from inch to metric.

Page 8-101, Figure 8-19. A1 Main Assembly Schematic Diagram:

2438A

>Change A1 (05005-60001) SERIES to 2438.

Page 8-103, Figure 8-20. A2 DVM Assembly Schematic Diagram:

2342A

>Change A2 (05005-60002) SERIES to 2342.
>Add R37 147K Resistor in series with the input to U4.
>Add R38 147K Resistor in series with HI Q GND.

Page 8-111, Figure 8-24. A8 HP-IB Interface Assembly:

2414A

>Change A8 (05005-60007) SERIES to 2414.

Active Components Table:
>Change U10 from 1820-2485 to 1820-3431.

WARNING

TO PROTECT YOUR UNIT UNDER TEST IT IS RECOMMENDED THAT THE USER LIFT THE PROBE TIP FROM THE CIRCUIT UNDER TEST WHEN MAKING CHANGES TO THE FRONT PANEL OF THE 5005B. DURING SOME FRONT PANEL OPERATIONS A ±10 VOLT, 38 MSEC, 50K OHM SOURCE IMPEDANCE TRANSIENT MAY OCCUR ON THE PROBE TIP. THE TRANSIENT MAY OCCUR ANY TIME FROM THE TIME THE KEY IS PRESSED TO SEVERAL SECONDS AFTER.